

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANT'S APPEAL BRIEF TRANSMITTAL LETTER

APPELLANT: Rainald SANDER DOCKET NO: P00,0184  
SERIAL NO.: 09/497,618 ART UNIT: 2814  
FILED: February 3, 2000 EXAMINER: D Farahani  
CONF. NO. 7717  
TITLE: TEMPERATURE-PROTECTED SEMICONDUCTOR SWITCH

5

Assistant Commissioner for Patents,  
Washington, D.C. 20231

10 Sir:

Appellants are submitting herewith, in triplicate, Appellants' Brief Under 37  
CFR 1.192 in support of the Notice of Appeal filed February 9, 2001. Also  
enclosed is a check for the \$320.00 fee required by 37 CFR 1.17(c). Please  
15 charge any additional fees which may be due and owing or credit any  
overpayment to Deposit Account No. 501519. A duplicate copy of this sheet is  
enclosed.

Submitted by,

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(Reg. No. 45,877)

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on March 26, 2003.

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Mark Bergner - Attorney for Applicants

## APPELLANT'S MAIN BRIEF ON APPEAL

TITLE: TEMPERATURE-PROTECTED SEMICONDUCTOR SWITCH

10 Sir:

20 was filed on January 31, 2003.  
RWSE1 00000014 09497618

The real party in interest in this appeal is the assignee, Infineon Technologies AG, a German corporation, by virtue of an assignment executed June 26, 2000 and recorded on July 17, 2000 at reel/frame: 010978 / 0876.

**RELATED APPEALS AND INTERFERENCES:**

There are no related appeals and no related interferences known to Appellant, Appellant's Assignee, or Appellant's legal representative.

**STATUS OF CLAIMS:**

5        Claims 1-9 are on appeal, and constitute all pending claims of the application. In paragraph 2 of the OA, the claims were rejected under 35 U.S.C. §102 and §103 based on prior art as follows:

Claims / Section	35 U.S.C. Sec.	References / Notes
1,2,4,6-8, 9	§102(b) Anticipation	<ul style="list-style-type: none"><li>• Yamaguchi, et al. (U.S. Patent No. 5,500,547).</li></ul>
3,7	§103(a) Obviousness	<ul style="list-style-type: none"><li>• Yamaguchi, et al. (U.S. Patent No. 5,500,547); and</li><li>• Roth, Fundamentals of Logic Design (1992).</li></ul>

10        Claim 5, while indicated as rejected in the OA, was not addressed in any portion of the detailed action—thus, Appellant is uncertain as to the status of this claim.

Copies of Yamaguchi, Roth, Pages, et al. (U.S. Patent No. 6,373,100) and Yabusaki, et al. (U.S. Patent No. 5,107,216) (the latter two being art cited by the  
15 Examiner for certain assertions made) are attached as Appendix C.

**STATUS OF AMENDMENTS:**

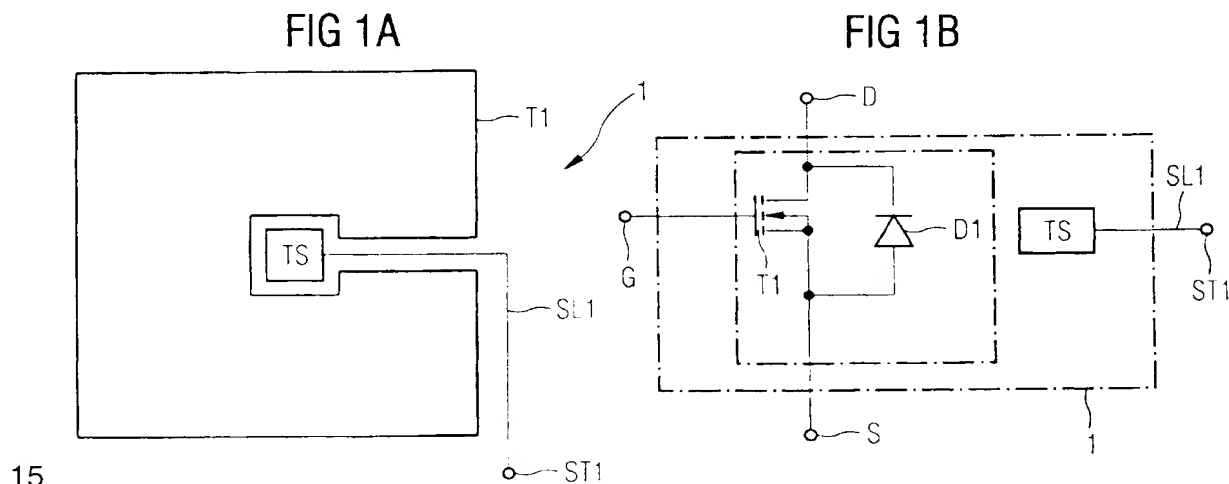
No amendments have been entered in this case. All claims presented are those originally filed.

**SUMMARY OF THE INVENTION:**

20        In general terms, the present invention is a temperature-protected

semiconductor switch that has both a temperature sensor configured to output a first signal, and a charge carrier detector configured to output a second signal. These two signals can be used to provide an accurate indication of when a true overtemperature situation occurs at the switch or whether a false positive  
 5 overtemperature situation has been triggered by the presence of problematic free charge carriers.

It is known to provide power switches with integrated temperature sensors to prevent thermal overload. These temperature sensors acquire the temperature of the power switch and convert this into a temperature-dependent  
 10 analog signal which then can be interpreted in an evaluation circuit—the circuit can then be used to shut off the semiconductor switch when a predetermined temperature has been exceeded. p. 1, 2nd ¶. Figures 1A and 1B below of the application illustrate such a known configuration. An exemplary switch element T1 that is a MOSFET is shown below. p. 2, first carryover ¶.



*Figs. 1A & 1B  
 Known Switch with Temperature Sensor*

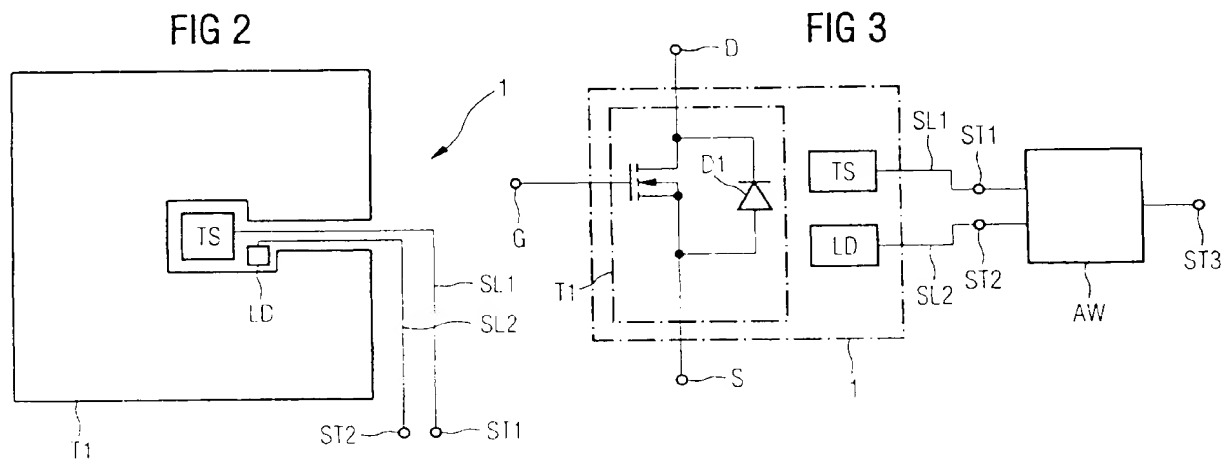
MOSFET-type switches often include a reverse diode D1 that is integrated

with the switch in a semiconductor body—however, when operated in a certain manner, this diode produces free charge carriers. These free charge carriers are problematic, however, because they can induce the temperature sensor TS to trigger a false positive overtemperature when no such overtemperature is  
5 present. p. 2, 2nd ¶.

One known solution that has been provided is to provide a charge carrier diffusion ring around the temperature sensor (see the ring around TS in Fig. 1A) that can block the free charge carriers and thus prevent false positive overtemperatures. Unfortunately, in order for the ring to adequately block  
10 (capture) the problematic charge carriers from the temperature sensor TS, this ring would have to be implemented very broadly (large), meaning that the temperature sensor TS would be located far away from the hottest location of the switch that is to be protected (and thus, have too slow of a reaction time to signal shutting the switch off). But if the temperature sensor is located close to the  
15 switch to improve reaction time, then the protective ring cannot sufficiently block the free charge carriers, thus increasing the probability of false positive overtemperature conditions by the temperature sensor. p. 3, first carryover ¶.

The invention addresses this problem by providing a charge carrier detector that provides an additional signal that can be used to protect the switch.  
20 p. 3, 2nd full ¶. The charge carrier detector permits the temperature sensor to be located near the switch, but the charge carrier detector provides information that permits one to distinguish between a temperature sensor signal due to a true overtemperature situation and a false overtemperature sensor signal triggered by the charge carriers. p. 3-4, last/first carryover ¶. Refer to the exemplary

embodiment illustrated below.



*Figs. 2 & 3*  
*Exemplary Embodiment of the Invention*

It can be seen from Figs. 2 and 3 that the charge carrier detector LD connects to a line SL2 via which a second signal can be output when the free charge carriers are detected. When the temperature sensor TS is triggered, it may be either because of a true overtemperature condition or because of the problematic charge carriers. If the signal from the charge carrier detector LD is present, then one can presume that the overtemperature signal provided by the temperature sensor TS is erroneous and not shut down the switch T1.

#### **ISSUES:**

The issues on appeal are as follows:

1. Whether the subject matter of claims 1-2, 4-6, 8 and 9 are anticipated by Yamaguchi (U.S. Patent 5,500,547); and
2. Whether the subject matter of claims 3 and 7 is obvious in view of Yamaguchi over Roth, Fundamentals of Logic Design, 1992.

### **GROUPING OF CLAIMS:**

The claims on appeal include one independent claim (claim 1) and eight dependent claims (2-9).

#### **Group 1: claims 1, 2, 8 and 9**

5        The primary basis of dispute for the rejection revolves around elements of independent claim 1. Appellant groups dependent claims 1, 2, 8, and 9 in the group with claim 1.

#### **Group 2: claims 4-6**

Appellant believes that dependent claims 4-6 are separately patentable,  
10 and thus places them in a second group for appeal. These claims are separately patentable because they address issues relating to the relative locations of the temperature sensor as well as the charge carrier detector. There mere presence of a charge carrier detector according to claim 1 is advantageous, but certain advantages could be realized in even a conventional placement of the  
15 temperature sensor away from the switch. Thus, it is additionally significant to locate the temperature sensor and charge carrier detector in certain locations as these locations permit better operability, smaller size and other cost to performance benefits.

#### **Group 3: claims 3 and 7**

20        Appellant believes that dependent claims 3 and 7 are separately patentable, and thus places them in a third group for appeal. These claims are separately patentable since they require the presence of a logic element that relates the first and second signals to the actions of determining whether to



protect the switch or not. There mere presence of a charge carrier detector according to claim 1 is advantageous, but how to utilize the signal originating with the charge carrier detector provides operational advantages to the circuit that are not present with the charge carrier detector or its appertaining signal alone.

5 **ARGUMENTS:**

***ARGUMENT 1—Anticipation by Yamaguchi of Claim 1 (and other dependent claims)***

***Examiner's Position: Claim 1 is anticipated by Yamaguchi because each of the elements, primarily the switch element, the temperature sensor (and its  
10 generated first signal), and the charge carrier detector (and its generated second signal), are all disclosed by Yamaguchi.***

In the OA, p. 2, the Examiner states, as a complete discussion for anticipation by Yamaguchi:

15           Regarding claim 1, in figures 3 and 4, Yamaguchi discloses a semiconductor device, 4A, and a MOS transistor 13 in parallel with the temperature sensing circuit 20, same circuit neutralizing the accumulated charge, in an N type body substrate 1.

          This language was carried over from a prior Office Action (dated May 29,  
20 2002). Appellant notes that in the Interview Summary, the Examiner indicates:

25           The limitation in claim 1, "a semiconductor switch element formed of a plurality of cells connected in parallel and including an integrated reverse diode", was discussed as [sic: to] where in the reference it could be found. Examiner explained that a diode can act as a switch, and therefore, diodes 22 and 21 of figure 4B, which are part of temperature sensor 20, comprise a switch.

          Although the Examiner had only referenced Yamaguchi's Fig. 4A with  
30 respect to claim 1 in the last Office Action, the Examiner referenced Fig. 4B

during the telephone interview in order to find all of the elements present in claim 1. Thus, although not corrected or clarified in the final OA, it is Appellant's understanding that the Examiner is equating the Yamaguchi disclosure to the elements of claim 1 of the present invention as follows, referring to Fig. 4B of Yamaguchi.

Claim 1 element	Yamaguchi
Charge carrier detector generating a second signal when free charge carriers are present in the semiconductor body	FET 13
Semiconductor switch element formed of a plurality of cells connected in parallel and including an integrated reverse diode	Diode element 22 + one or two of the three diodes 21
Temperature sensor that generates a first signal given the occurrence of an excess temperature	all three diode elements 21 + diode 22 combined (overall element 20)

In response to Appellant's assertion that it was improper to equate the diode element combination 21, 22 as the switch of the present invention, the Examiner cited Yabusake, U.S. Patent No. 5,107,216, Fig. 9 and 6/20-37 as suggesting that the diode combination 21, 22 can be construed as a switch.

In response to Appellant's assertion that it was improper to equate the FET transistor as being the carrier charge detector, the Examiner cited Pages, et al., U.S. Patent 6,373,100 at 5/5-15 that an FET outputs a signal in response to the appearance of free charge carriers in a semiconductor body.

In response to Appellant's assertion that the Examiner was equating an identical element of Yamaguchi with both the present invention's "switch" and

"temperature sensor" (effectively ignoring a separately called out element of the present invention), the Examiner replied that [in Yamaguchi, Fig. 4B] element 20 (made up of diode 22 and diodes 21) constituted the temperature sensor and that diodes 21 and 22 act as a switch element, and that therefore the temperature  
5 sensor and the switch are not the same element. OA, p. 4, ¶1.

In response to Appellant's assertion that if the elements of Yamaguchi are applied as the table above indicates, the temperature sensor would have to protect part of itself, (since the switch would have to be a part of the temperature sensor), the Examiner replied that in Yamaguchi, "element 20 lets out the extra  
10 current that may occur in it self [sic: itself] (the reference actually states that circuit as a whole prevents damage to its individual diodes in an event of extraneous current, hence temperature). See column 5, lines 38-43". OA, p. 4, ¶2.

Finally, in response to Appellant's assertion that the present invention  
15 requires two signals to be output in the claimed invention, the Examiner asserted that element 20 in Yamaguchi [Examiner equated to temperature sensor] lets out the extra current, or signal, and that furthermore, that Pages has the FET outputting a current, or signal, in response to the presence of charge carriers in a semiconductor body.

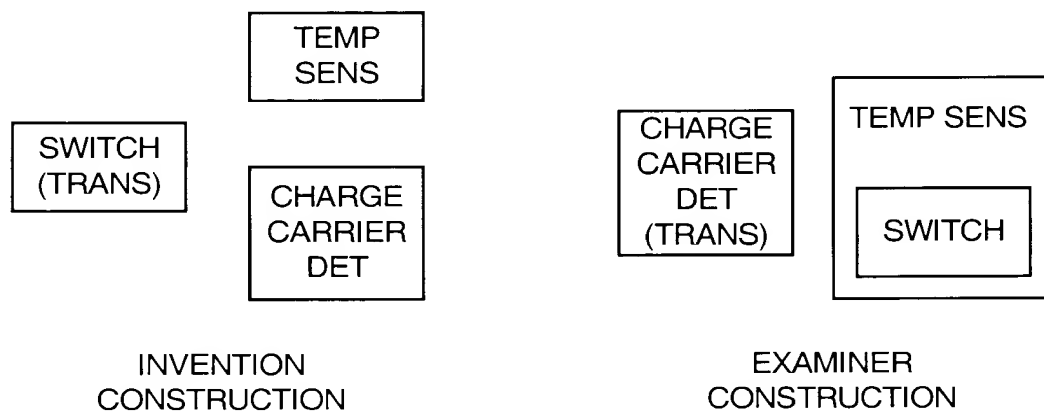
20 ***Appellant's Position: The Examiner has misconstrued the elements of the claim, and has ignored various elements, their relationships and functions in forcing the Yamaguchi reference to improperly read on elements of claim 1 of the present invention.***

The present invention requires the presence of four elements (the

semiconductor body, the semiconductor switch, the temperature sensor, and the charge carrier detector) and requires the prescribed interrelationship as described in the claims, namely that the switch element, the temperature sensor, and the charge carrier detector are all separate elements. The switch and the temperature sensor are separate from one another, but they are both integrated into the semiconductor body. Yamaguchi lacks a teaching of these four elements in the prescribed relationship according to claim 1 and thus cannot anticipate the present invention. The present invention's use of all of these elements presents an advantageous architecture and functionality over the invention disclosed by Yamaguchi.

Appellants believe that the Examiner has misconstrued the disclosure of Yamaguchi and provided inconsistent definitions in equating elements of Yamaguchi that read on elements of the present invention.

The following diagram illustrates the invention as construed by the Appellant on the left, and the construction of the Yamaguchi reference by the Examiner on the right.



1. Claim 1 of the present invention separately calls out the switch element and the temperature sensor element, and the Examiner has improperly combined the two.

In the OA, p. 4, 1st ¶, the Examiner indicates that "element 20 in Yamaguchi is a temperature sensor, and diodes 21 and 22 act as a switch element. Therefore, the temperature sensor and the switch are not the same element."

In Yamaguchi, element 20 of Fig. 4B is identified at 4/65-67 (referring to Fig. 4A, but presumably applying to 4B as well) as a temperature sensor. The individual part shown in FIG. 4A includes one FET 13 and one directional circuit 20 biased for sensing a peripheral temperature of the FET13. Thus, Appellant does not disagree with the Examiner's characterization of diode elements 21 + 22 combined (element 20) being equated to the temperature sensor of the present invention.

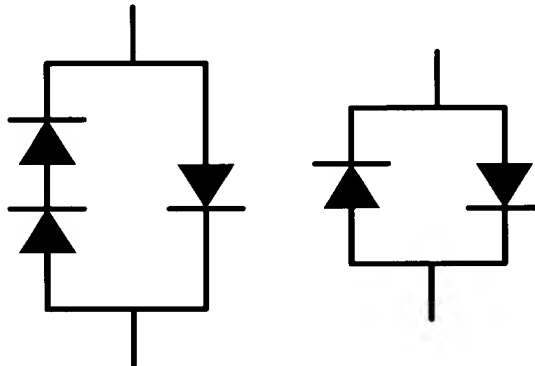
However, when the Examiner indicates that [a subset of] diodes 21 and 22 act like a switch element, this would require the switch to be a part [or a subset] of the temperature sensor itself. The switch element in the present invention is called out as a separate element and is not a part of the temperature sensor. The only relationship provided in the present invention, according to claim 1 is that both "the semiconductor switch element and the temperature sensor are integrated together in the semiconductor body". Nowhere is a relationship of the switch being a part of the temperature sensor called out in any of the claims. The Examiner is inappropriately reading this construction into the claim language.

2. The Examiner's construction of the diodes as a switch is improper and is not how one would normally construe a switch in the field of temperature

sensing circuits for protecting switches, since Yamaguchi, as art in the field, construes the FET as the switch and not a subset of the temperature sensing diodes..

The Examiner is equating at least one of the following constructions in

5 Yamaguchi's Fig. 4B as being a "switch".



The Examiner cited to Yabusaki, Fig. 9 and 6/20-37 as showing such a diode construction being considered a "switch"—Appellants see no such disclosure. The Yabusaki reference does not use the word "switch" at all in this  
10 passage, and simply refers to the fact the paired diodes can be in states of conductive and non-conductive based on the applied voltage. There is no sense of control that is associated with the notion of a "switch" in this configuration.

During the telephone interview, the Examiner indicated that these devices can operate as a switch by virtue of the fact that they can be in a state of being  
15 "on" and "off" depending on voltages and polarity provided. Appellants assert that this definition is too broad, that mere conducting and non-conducting is insufficient to form a "switch"—and Appellants see no definition of a "switch" provided by the Examiner that permits such a broad definition.

But even if, for the sake of argument, the Examiner's diode pair could be

construed as a "switch" in a particular field of the art, such a definition is not how one of ordinary skill in the art would construe it in the field of temperature protected switches.

In this field of art, Yamaguchi clearly indicates the operation of FET 13 as the switch element at 5/25-27, "[the voltage drop] is detected at the detection end to provide a temperature signal to the FET control signal, where it is processed to **turn off the FET 13** if the signal represents a critical temperature" [emphasis added]. Thus, the switch in Yamaguchi is provided with a control that is utilized to turn off the switch in response to a temperature signal. Nowhere in Yamaguchi can a teaching of the diodes according to the above structure acting as a switch be found. In fact, Yamaguchi represents the specific type of construction as that which is acknowledged by the present application as prior art—i.e., the presence of a temperature sensor protecting a switch, without a charge carrier detector.

3. The Examiner has inconsistently defined what constitutes the switch in the present invention, in that he equates the present invention's switch to Yamaguchi's diodes, as described above, and also to Yamaguchi's FET (which he has already defined as the charge carrier detector).

As noted above, the Examiner has indicated that the present invention's switch is shown by Yamaguchi's diodes 21 and 22. However, in the OA on p. 2 last full ¶, the Examiner states:

Regarding claim 6, Yamaguchi discloses a temperature signal produced by circuit 20, figure 4B, to be provided to the FET control signal, which consequently turns off the FET 13. The charge carrier neutralizing diode 22 is adjacent to the temperature signal.

The fact that the temperature signal "turns off" FET 13 indicates that the Examiner is now considering Yamaguchi's FET as being the switch, and not the diodes. This represents an inconsistent position on how the elements of Yamaguchi are being read on the present invention and this inconsistency is  
5 impermissible under 35 U.S.C §102.

Furthermore, the Examiner states on page 2 of the OA in the second ¶  
under section 2,

10                   Regarding claim 1, in figures 3 and 4, Yamaguchi  
discloses a semiconductor device, 4A, **and a MOS  
transistor 13 in parallel with the temperature  
sensing circuit 20**, same circuit neutralizing the  
accumulated charge, in an N type body substrate 1.

The only place "parallel" is used in the present invention's claim 1 is to  
describe the structure of the semiconductor switch element—the Examiner  
15 clearly indicates the presence of Yamaguchi's MOS transistor 13 in describing  
the "parallel" structure. Clearly the Examiner originally interpreted the MOS  
transistor 13 of Yamaguchi with being the "switch", which is consistent with  
Yamaguchi's own description of the device's operation.

20                   4. The Examiner has incorrectly construed the FET 13 of Yamaguchi as  
inherently operating as the charge carrier detector of the present  
invention.

In the prior Office Action, dated May 29, 2002, the Examiner stated on p.  
4, paragraph 9, that:

25                   The applicant argues that [sic: the] Yamaguchi  
reference does not teach a device that produces the  
two [sic: two] signals of the disclosed claimed  
invention. This is not persuasive, since it is an  
inherent function of MOS transistor 13 to create a  
signal in the event of free charge carrier occurrence.



Furthermore, temperature sensor 20 will generate a second signal.

When challenged by Appellant to provide a disclosure indicating the operation of the MOS transistor 13 as a charge carrier detector, the Examiner, in  
5 the current OA, p. 4, last two paragraphs:

Regarding applicant's request for some kind of reference to show the inherency of a FET being a charge carrier detector, the reference is provided below in the Prior Art of Record section....  
10 Furthermore, as indicated in paragraph 2 of the Prior Art of Record section (as disclosed in the Pages et al.), a FET outputs a current, or signal, in response to the presence of charge peers in a semiconductor body.

15 This Prior Art of Reference section cited by the Examiner in the OA, p. 5, 2nd ¶ indicates that Pages, at 5/5-15 describes an FET transistor acting as a carrier charge detector (i.e., it outputs a signal in response to the appearance of free charge carriers in a semiconductor body).

The portion of Pages cited by the Examiner does not address the use of  
20 an FET as a charge carrier detector, as defined by the present invention, but only identifies that charge carriers (i.e., electrons) flow from a source region into a substrate. Such a broad reading of Pages would infer that any semiconductor device is a "charge carrier detector" because, when they operate, they all have electrons flowing through them. And the Examiner's characterization of  
25 "detection" seems to be broad enough to encompass any device through which current flows, including wire.

The present invention is not concerned with a detector that simply detects charge carriers flowing through itself—rather it is concerned with detecting

charge carriers that are external to itself. That is the point of the present invention, i.e., that a charge carrier detector detects charges that could trigger a false positive overtemperature reading in a temperature sensor. The Examiner has not explained how Pages provides a role of "detection".

5           In summary, the present invention requires the presence of four elements (the semiconductor body, the semiconductor switch, the temperature sensor, and the charge carrier detector) and requires the prescribed interrelationship as described in the claims. Yamaguchi lacks a teaching of these four elements and their respective relationships to one another and thus cannot anticipate the  
10 present invention. The present invention's use of all of these elements presents an advantageous architecture and functionality over the invention disclosed by Yamaguchi.

          For this reason, Appellant believes that an element required by claim 1 is not found in Yamaguchi and thus Yamaguchi cannot be said to anticipate the  
15 present invention. Since all remaining claims depend from claim 1, Appellant respectfully request that the Examiner's §102 rejection be reversed in the present application.

**ARGUMENT 2—Anticipation by Yamaguchi of Claims 4 and 6**

**Examiner's Position:** Claim 4 is anticipated by Yamaguchi showing a pair of adjacent diodes for sensing the temperature and for the accumulated charge. Claim 6 is anticipated by Yamaguchi showing a temperature signal  
5 produced by the circuit to be provided to the FET control signal, which turns off the FET. The charge carrier neutralizing diode is adjacent to the temperature signal.

In the OA, p. 2, the Examiner states:

10           Regarding claim 4, Yamaguchi discloses the pair of adjacent diodes 20, for sensing the temperature and for the accumulated charge, 21 and 22 of figure 4A.  
15           Regarding claim 6, Yamaguchi discloses a temperature signal produced by circuit 20, figure 4B, to be provided to the FET control signal, which consequently turns off the FET 13. The charge carrier neutralizing diode 22 is adjacent to the temperature signal.

**Appellant's Position:** As to claim 4, the pair of diodes 20 do not serve for the sensing of temperature and for the sensing for the accumulated charge,  
20 21 and 22 of Figure 4A because these Yamaguchi only describes these as a temperature sensor. As to claim 6, Yamaguchi does not show a charge carrier detector positioned adjacent a signal line of the temperature sensor leading out of the semiconductor switch.

In Yamaguchi, element 20 of Fig. 4B is identified at 4/65-67 (referring to  
25 Fig. 4A, but presumably applying to 4B as well) as a temperature sensor.

However, Yamaguchi does not disclose that the arrangement 20 or any part thereof operates as a charge carrier detector. As noted above, Yamaguchi represents known prior art of a switch protected by a temperature sensor, but that does not have a charge carrier detector.

30           The Examiner asserted, in addressing claim 1, that Yamaguchi's FET

acted as the charge carrier detector in the circuit, but under claim 4 here is asserting that some portion of the diodes 20 serves as the charge carrier detector, reflecting an inconsistency in applying the Yamaguchi reference to the present invention.

5           With respect to claim 6, Appellants note the above argument that the Examiner equates the FET as being the switch under this claim, but equates some portion of the diodes 20 as being the switch in applying Yamaguchi to the parent claim 1. This is impermissible under 35 U.S.C. §102—elements of a prior art reference cannot be applied inconsistently in order to show anticipation.

10 Furthermore, Yamaguchi never discusses a charge carrier detector nor how such a mechanism would be positioned adjacent a signal line of the temperature sensor.

***ARGUMENT 3—Obviousness of Claims 3, 7 over Yamaguchi in View of Roth***

***Examiner's Position: Claims 3 and 7 are obvious over Yamaguchi and Roth***

15 ***because Roth discloses a well known logic function of providing an exclusive-or logic gate.***

The Examiner indicates that in addition to Yamaguchi, as applied to the other claims as anticipating art, Roth discloses the use of an exclusive-or logic gate, and thus it would have been obvious to combine Yamaguchi and Roth to

20 arrive at the evaluator means element of both claims 3 and 7.

***Appellant's Position: The Examiner does not provide any evidence of a teaching or suggestion to combine the references, nor would the cited function described by the Examiner work in the present invention.***

The Examiner cites Roth as describing an exclusive-or function that

obviates the present invention. However, the present invention would not work properly if the exclusive-or function were used.

According to the Specification on p. 6, the evaluator means checks to see if the temperature sensor signal is high. If so, a check is made to see if the  
5 charge carrier detector is high as well. If it is, this signals a false positive from the temperature sensor (i.e., caused by the presence of spurious charge carriers and not by a true overtemperature)—the output of the evaluator is low and no further action is taken.

If, however, the temperature sensor signal is high, and the charge carrier  
10 detector is low (indicating no problematic spurious charge carriers are present), then this reflects a true overtemperature condition and the output of the evaluator means is high, which triggers a switch shut-off mechanism.

In the exclusive-or example cited by the Examiner, if the temperature sensor provided a low output, and the charge carrier detector provided a high  
15 output, this situation would be indistinguishable by the exclusive-or gate from a true overtemperature situation and would thus produce a high evaluator signal that would act to signal a cutting-off of the switch when no overtemperature situation existed.

Furthermore, with respect to the Examiner's construction of the  
20 Yamaguchi elements described above, in which the switch is a part of the temperature sensor, the Examiner has not indicated how a signal of the temperature sensor could possibly be separated from a signal produced by the switch itself, which would be a significant issue if Yamaguchi's elements are to

read on the elements of the present invention as indicated by the Examiner.

A significant feature of the invention as claimed in claim 1 is providing the two signals from the device, with the first signal originating from the temperature sensor and the second signal originating from the charge carrier detector, the  
5 charge carrier detector being a separate element from the semiconductor switch. This architecture provides structural and functional advantages that are not taught or suggested by Yamaguchi and Roth, either alone or in combination.

For these reasons, Appellant asserts that the claim language clearly distinguishes over the prior art, and respectfully request that the Board reveres  
10 the Examiner with respect to the 35 U.S.C. §103(a) rejection.

**CONCLUSION:**

For the above reasons, Appellants respectfully submits that the Examiner is in error in law and in fact in rejecting claims 1-9 based on the teachings of the above-discussed references. Reversal of the rejection of all of those claims is  
5 justified, and the same is respectfully requested.

This Brief is accompanied by a check in the amount of \$320.00, as required by 37 C.F.R. §1.17(c). If necessary, the Commissioner is hereby authorized to charge any additional fees which may be required to account No. 501519.

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Respectfully submitted,

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\_\_\_\_\_(Reg. No. 45,877)

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25 being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on March 26, 2003.

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\_\_\_\_\_  
Mark Bergner

**APPENDIX A**  
**CLAIMS INVOLVED IN THE APPEAL**

1. (original) A temperature-protected semiconductor switch, comprising:
- 5 a semiconductor body of first conductivity type;
- a semiconductor switch element formed of a plurality of cells connected in parallel and including an integrated reverse diode;
- a temperature sensor which generates a first signal given the occurrence of an excess temperature, wherein the semiconductor switch
- 10 element and the temperature sensor are integrated together in the semiconductor body; and
- a charge carrier detector that generates a second signal given the occurrence of free charge carriers in the semiconductor body.
- 15 2. (original) A temperature-protected semiconductor switch as claimed in claim 1, further comprising:
- a parasitic component formed between the charge carrier detector, the semiconductor body and at least one cell of the semiconductor switch element.
- 20 3. (original) A temperature-protected semiconductor switch as claimed in claim 1, further comprising:
- in evaluation means, wherein the first and second signals are supplied to the evaluation means and logically operated with one another
- 25 thereat for indicating an unambiguous excess temperature in the semiconductor switch element.



4. (original) A temperature-protected semiconductor switch as claimed in claim 1, wherein the charge carrier detector is positioned adjacent the temperature sensor.

5 5. (original) A temperature-protected semiconductor switch as claimed in claim 1, wherein the temperature sensor is attached proximate a hottest location of the semiconductor body

6. (original) A temperature-protected semiconductor switch as claimed in  
10 claim 1, wherein the charge carrier detector is positioned adjacent a signal line of the temperature sensor leading out of the semiconductor switch.

7. (original) A temperature-protected semiconductor switch as claimed in claim 3, wherein the evaluation means is monolithically integrated with the  
15 semiconductor switch.

8. (original) A temperature-protected semiconductor switch as claimed in claim 1, further comprising:

20 at least one of a bipolar transistor and a thyristor as the temperature sensor.

9. (original) A temperature-protected semiconductor switch as claimed in claim 1, wherein the first conductivity type is n-conductive.

**APPENDIX B  
FINAL OFFICE ACTION  
AND  
TELEPHONE INTERVIEW**



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/497,618	02/03/2000	Rainald Sander	POo,0184	7717

7590 11/06/2002

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EXAMINER

FARAHANI, DANA

ART UNIT PAPER NUMBER

2814

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**RECEIVED**

NOV 12 2002

SCHIFF HARDIN & WAITE  
U.S. PATENT DEPT.

## Office Action Summary

Application No.

09/497,618

Applicant(s)

SANDER, RAINAL

Examiner

Dana Farahani

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on 03 September 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☐ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4, 6-8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamaguchi et al., hereinafter Yamaguchi, previously cited.

Regarding claim 1, in figures 3 and 4, Yamaguchi discloses a semiconductor device, 4A, and a MOS transistor 13 in parallel with the temperature sensing circuit 20, same circuit neutralizing the accumulated charge, in an N type body substrate 1.

Regarding claim 2, Yamaguchi discloses the diodes for neutralizing the accumulated charge and sensing the temperature, and the MOS transistor component in the semiconductor body. Note figure 3, number 13 and 20.

Regarding claim 4, Yamaguchi discloses the pair of adjacent diodes 20, for sensing the temperature and for the accumulated charge, 21 and 22 of figure 4A.

Regarding claim 6, Yamaguchi discloses a temperature signal produced by circuit 20, figure 4B, to be provided to the FET control signal, which consequently turns off the FET 13. The charge carrier neutralizing diode 22 is adjacent to the temperature signal.

Regarding claim 8, Yamaguchi discloses thyristor 20 as a temperature sensor.

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Regarding claim 9, Yamaguchi discloses an N+ type silicon body substrate, paragraph 1 line 7.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi as applied to claims 1, 2, 4-6, 8 and 9, above, and further in view of Roth, previously cited.

It is well known in the art that an exclusive-or logic gate outputs 1, or H, when one of its inputs is 0, or L, and the other input is 1, or H. (see, for example, Roth, page 51). Therefore it would have been obvious to one of ordinary skills in the art at the time the invention was made to use an exclusive-or logic gate in Yamaguchi to get an output signal corresponding to the temperature and charge carrier input signals.

### ***Response to Arguments***

5. Applicant's arguments filed 9/3/02 have been fully considered but they are not persuasive.

Regarding applicant's request of a reference to show that a two-diode configuration is a switch, see Prior Art below.

Applicant's argument that "... Examiner would be equating an identical element of Yamaguchi with both the present invention's switch and temperature sensor" is not found persuasive, since element 20 in Yamaguchi is a temperature sensor, and diodes 21 and 22 act as a switch element. Therefore, the temperature sensor and the switch are not the same element.

Applicant further argues that since the switch is part of the temperature sensor how it can be protected. Note that element 20 lets out the extra current that may occur in it self (the reference actually states that circuit 20 as a whole prevents damage to its individual diodes in an event of extraneous current, hence temperature. See column 5, lines 38-43.

Regarding applicant's request for some kind of reference to show the inherency of a FET being a charge carrier detector, the reference is provided below in the Prior Art of Record section.

Finally, applicant argues that there are two signals in the claimed invention, that is first and second signals from the temperature sensor and charge carrier detector, respectively. Note, that element 20 in Yamaguchi lets out the extra current, or signal. Furthermore, as indicated in paragraph 2 of the Prior Art of Record section (as disclosed in Pages et al.), a FET outputs a current, or signal, in response to the presence of charge carriers in a semiconductor body.

### ***Prior Art of Record***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See, for example, U.S. Patent 5,107,216, issued to Yabusaki et al., wherein is sated the two diode configuration in figure 9 act as a switch (see column 6, lines 20-37). Also, see U.S. Patent 6,373,100, issued to Pages et al., wherein is stated in column 5, lines 5-15, that a FET transistor acts as a carrier charge detector (that is it outputs a signal in response to appearance of free charge carriers in a semiconductor body).

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.




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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani  
October 30, 2002



LONG PHAM  
PRIMARY EXAMINER

**Notice of References Cited**

Application/Control No.

09/497,618

Applicant(s)/Patent Under  
Reexamination  
SANDER, RAINALD

Examiner

Dana Farahani

Art Unit

2814

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number	Date	Name	Classification	
		Country Code-Number-Kind Code	MM-YYYY			
	A	US-5,107,216	04-1992	Yabusaaki et al.	324	318
	B	US-6,373,100	04-2002	Pages et al.	257	343
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

**FOREIGN PATENT DOCUMENTS**

*		Document Number	Date	Country	Name	Classification	
		Country Code-Number-Kind Code	MM-YYYY				
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a) )  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
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Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/497,618	02/03/2000	Rainald Sander	POo.0184	7717

7590 09/12/2002  
Schiff Hardin & Waite  
Patent Department  
7100 Sears Tower  
Chicago, IL 60606-6473

EXAMINER

FARAHANI, DANA

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 09/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

RECEIVED  
SEP 17 2002  
SCHIFF HARDIN & WAITE  
US PATENT OFFICE

# Interview Summary

Application No.

09/497,618

Applicant(s)

SANDER, RAINAL

Examiner

Dana Farahani

Art Unit

2814

All participants (applicant, applicant's representative, PTO personnel):

(1) Dana Farahani.

(3) \_\_\_\_\_.

(2) Mark Bergner.

(4) \_\_\_\_\_.

Date of Interview: 26 August 2002.

Type: a) ☒ Telephonic b) ☐ Video Conference  
c) ☐ Personal [copy given to: 1) ☐ applicant 2) ☐ applicant's representative]

Exhibit shown or demonstration conducted: d) ☐ Yes e) ☒ No.  
If Yes, brief description: \_\_\_\_\_.

Claim(s) discussed: 1.

Identification of prior art discussed: Yamaguchi et al..

Agreement with respect to the claims f) ☐ was reached. g) ☒ was not reached. h) ☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: the limitation in claim 1, "a semiconductor switch element formed of a plurality of cells connected in parallel and including an integrated reverse diode", was discussed as where in the referee it could be found. Examiner explained that a diode can act as a switch, and therefore, diodes 22 and 21 of figure 4B, which are part of temperature sensor 20, comprise a switch.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

i) ☐ It is not necessary for applicant to provide a separate record of the substance of the interview(if box is checked).

Unless the paragraph above has been checked, THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

  
Examiner's signature, if required

## Summary of Record of Interview Requirements

### Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

#### Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

##### Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

##### 37 CFR §1.2 Business to be transacted in writing

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiner's Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case unless both applicant and examiner agree that the examiner will record same. Where the examiner agrees to record the substance of the interview, or when it is adequately recorded on the Form or in an attachment to the Form, the examiner should check the appropriate box at the bottom of the Form which informs the applicant that the submission of a separate record of the substance of the interview as a supplement to the Form is not required.

It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,  
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

#### Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

**APPENDIX C  
ART REFERENCES**



## Yamaguchi et al.

[45] **Date of Patent:** Mar. 19, 1996

- |           |        |            |           |
|-----------|--------|------------|-----------|
| 5,025,298 | 6/1991 | Fay et al. | 257/470   |
| 5,237,481 | 8/1993 | Soo et al. | 257/467 X |

- FOREIGN PATENT DOCUMENTS

- |           |         |             |         |
|-----------|---------|-------------|---------|
| 62-156850 | 7/1987  | Japan ..... | 257/470 |
| 62-229866 | 10/1987 | Japan       |         |

- Primary Examiner*—William Mintel

- [22] Filed: Dec. 27, 1994

- [30] Foreign Application Priority Data

- Dec. 28, 1993 [JP] Japan ..... 5-335188

- [51] Int. Cl.
- <sup>6</sup>
- ..... H01L 31/058

- [52] U.S. Cl. .... **257/359**; 257/362; 257/467;  
257/469; 257/470; 307/117; 307/651

- [58] **Field of Search** ..... 257/491, 467,  
257/469, 470, 379, 380, 381, 358, 359,  
363; 307/651, 117

- [56]
- References Cited**

## U.S. PATENT DOCUMENTS

- 4,896,199 1/1990 Tsuzuki et al. .... 257/470 X

[57] **ABSTRACT**

A two-way conductive directional circuit formed in a polycrystalline silicon layer separated by an insulation film from a semiconductive element is one-way biased for sensing a temperature of the semiconductive element. The directional circuit may be provided with a bias in either conductive direction thereof for sensing a temperature of the semiconductive element, before being provided with a bias in the other conductive direction thereof for sensing the temperature of the semiconductive element.

**4 Claims, 5 Drawing Sheets**

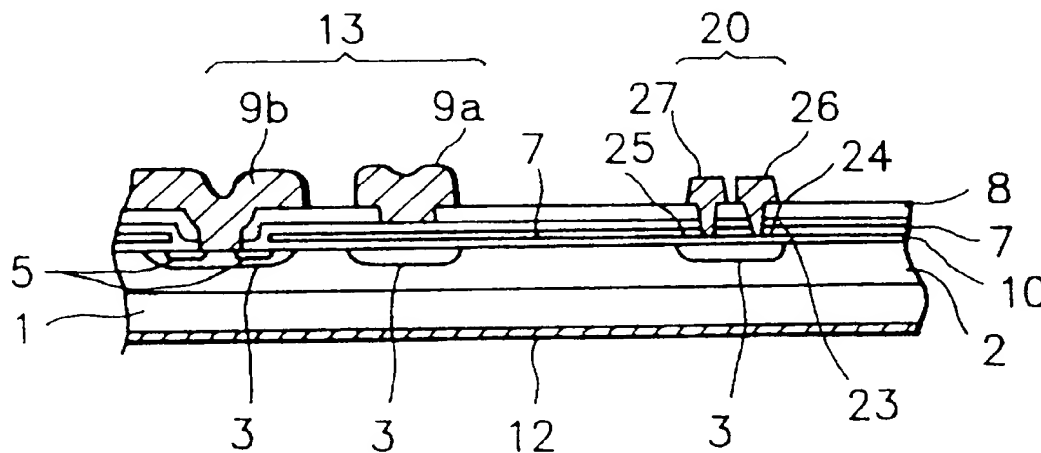


FIG. 1  
PRIOR ART

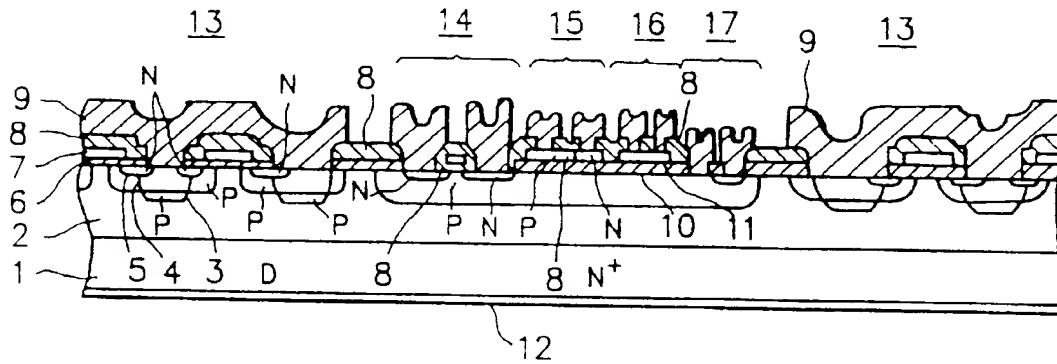
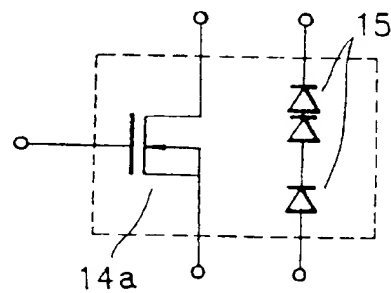
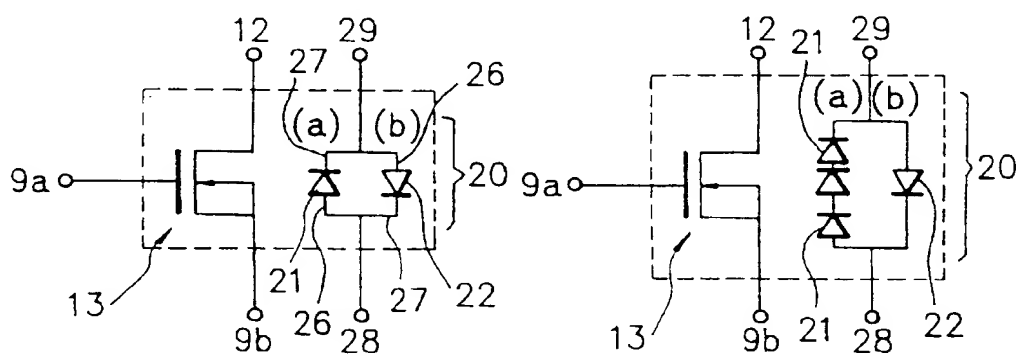


FIG. 2  
PRIOR ART

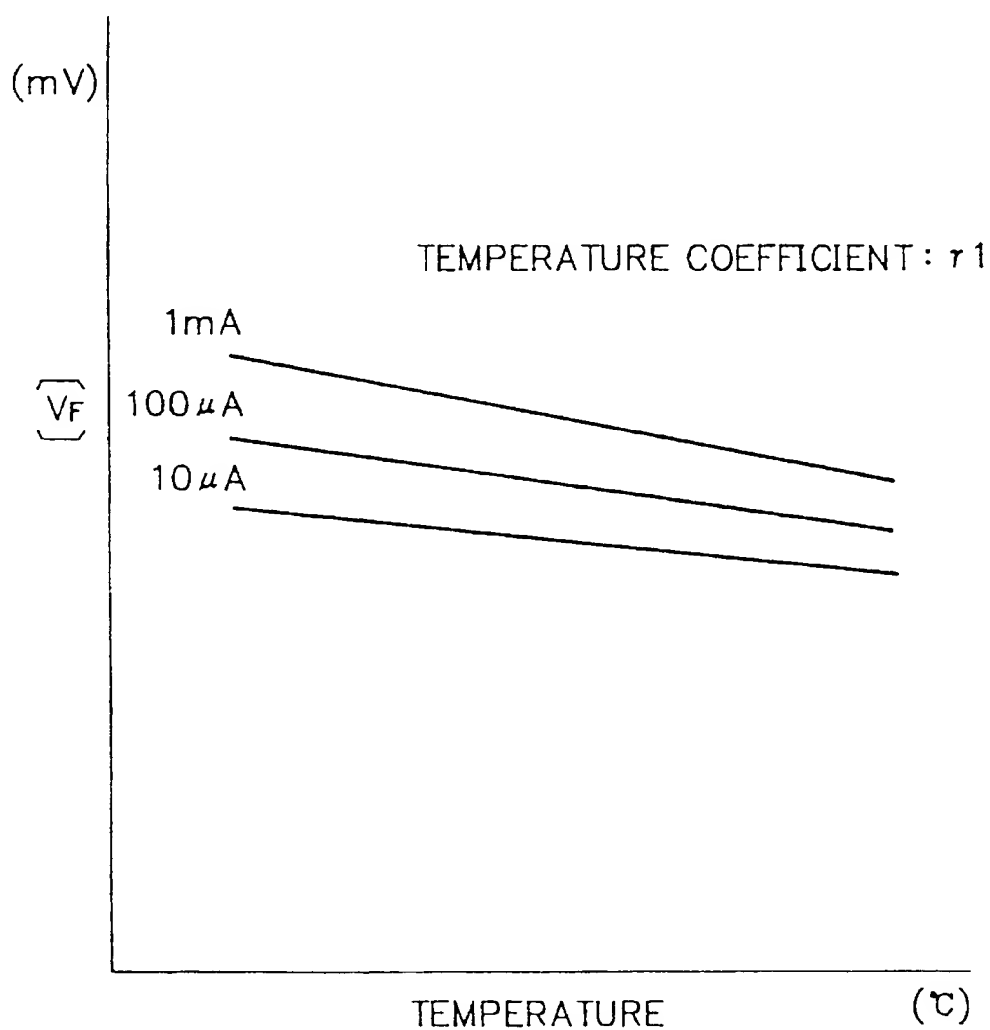






## FIG. 5

&lt; TEMPERATURE-VF &gt;

DIODE CONNECTION: 

## FIG. 6

< TEMPERATURE -  $V_F$  >

DIODE CONNECTION :

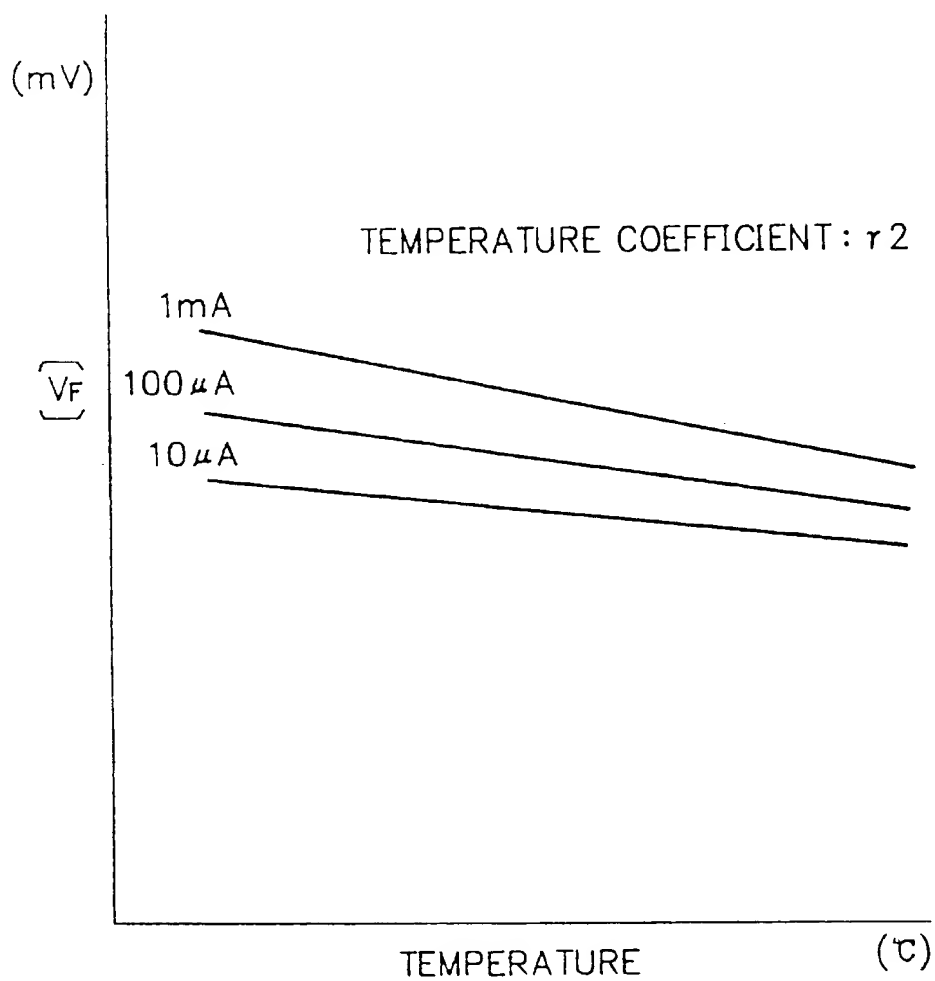
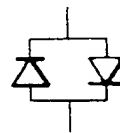
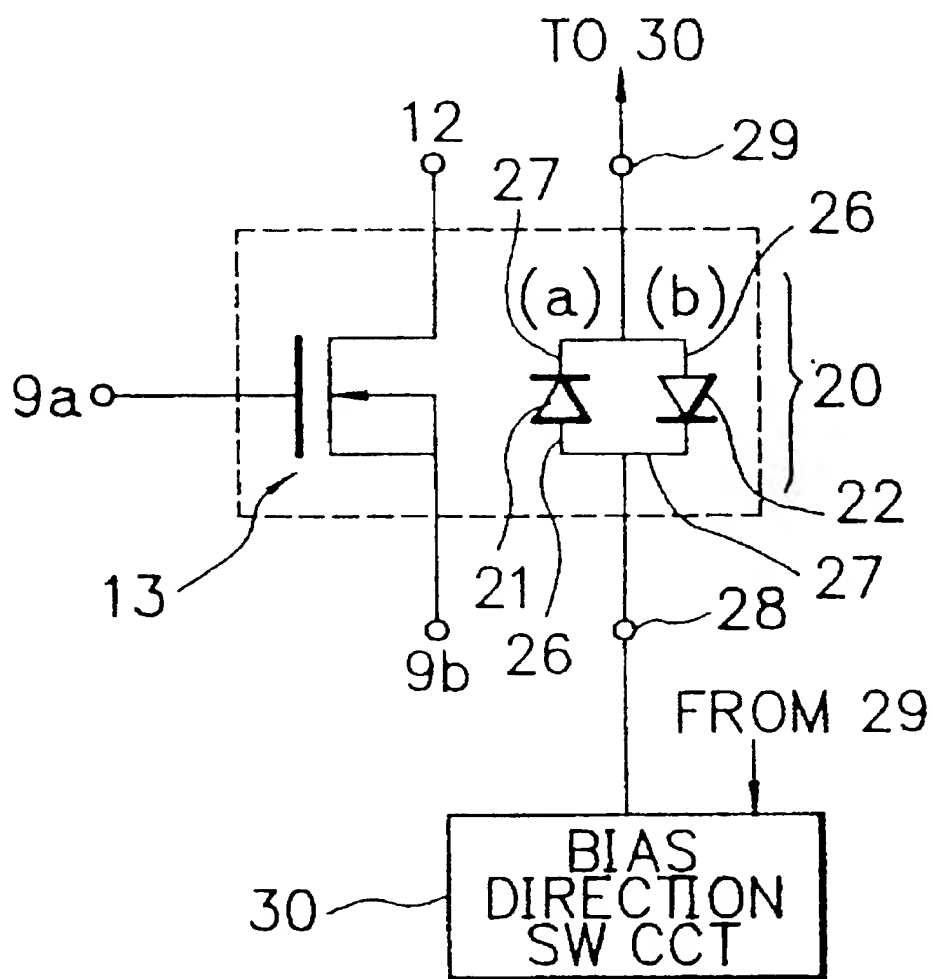


FIG. 7



# 1 INTEGRATED SEMICONDUCTOR DEVICE WITH TEMPERATURE SENSING CIRCUIT AND METHOD FOR OPERATING SAME

## BACKGROUND OF THE INVENTION

The present invention relates to an integrated semiconductor device capable of a temperature sensing of internal semiconductive elements, and a method for operating the same.

## DESCRIPTION OF THE RELATED ARTS

FIG. 1 shows a conventional integrated semiconductor device of such a type disclosed in Japanese Patent Laid-Open Publication No. 62-229866. As in FIG. 1, it has arrayed therein power MOS FETs 13, lateral MOS transistors 14 and polycrystalline silicon diodes 15, as well as polycrystalline silicon resistors 16 and constant voltage Zener diodes 17. It further includes an N<sup>+</sup> type silicon substrate 1, an N<sup>-</sup> type silicon epitaxial layer 2 formed on the substrate 1, and P type and N type diffusion layers 3 and 4 formed in the layer 2, respectively.

Moreover, it has a gate oxide film 6, a polycrystalline silicon layer 7, an interlayer insulating film 8, another insulation film 10, and a P<sup>+</sup> type diffusion layer 11, a drain electrode 12 and aluminum electrodes 9. Those members have the functions well-known in the art.

FIG. 2 is an equivalent circuit of an essential part of the semiconductor device that includes a MOS transistor 14 and a diode circuit for sensing a temperature of the transistor. The diode circuit consists of the diodes 15 connected in series.

When the semiconductor substrate has a normal temperature, that is, when the temperature at each junction element of an active semiconductive element is within a normal range, the semiconductive element operates normally. On the contrary, if the substrate temperature abnormally rises, that is, if the junction temperature is raised to be critical, the circuit of diodes 15 sensing the abnormal temperature rise gives a correspondent signal to a control circuit, which then forcibly stops operation of the semiconductive element, thereby preventing the element from being thermally damaged.

The conventional semiconductor device has a temperature sensing circuit formed therein which comprises the diodes 15 connected simply in series, as described. The series connection provides a relatively large temperature coefficient, permitting a facilitated temperature detection to be performed with an increased sensitivity.

However, it necessarily accompanies an withstand voltage at a cathode end of the circuit of diodes 15, which may cause a power breakdown of the diodes 15.

In particular, it thus is subjected to a reduced ESD (electrostatic discharge) durability between the cathode end and an anode end of the circuit of diodes 15.

In this connection, even a single diode circuit can provide a competent temperature coefficient, but is insufficient to always provide a required ESD durability for a current-day high integration.

In other words, undesirable electrostatic charges tend to accumulate at both ends of the diode circuit, as well known in the art, having an increasing electrostatic voltage developed thereacross to exert emfs (electromotive forces) on the charges that may destroy a temperature sensing diode.

## 2 SUMMARY OF THE INVENTION

The present invention has been achieved with such points in mind.

It is therefore a principal object of the present invention to provide an integrated semiconductor device having a temperature sensing circuit formed therein, permitting a competent temperature coefficient to be availed, without introducing a reduced ESD durability.

It also is an object of the present invention to provide a method for operating an integrated semiconductor device having a temperature sensing circuit formed therein, providing a relatively long service life in a simple manner.

To achieve the object, the present invention provides an integrated semiconductor device comprising a semiconductive element formed therein, an insulation film formed on the semiconductive element, a polycrystalline silicon layer formed on the insulation film, a two-way conductive directional circuit formed in the silicon layer, and the directional circuit being one-way biased for sensing a temperature of the semiconductive element.

According to the invention, in an integrated semiconductor circuit, a two-way directional circuit that is separated from a semiconductive element by an insulation film is adapted for sensing a temperature of the semiconductive element. The two-way conductive directional circuit should have a pair of one-way conductive circuits different from each other in conductive direction, so that either one-way conductive circuit may be one-way biased for sensing a temperature of the semiconductive element.

The sensing may be effected by use of a diode that can provide a competent temperature coefficient. Any tendency of charge accumulation is cancellable through the other one-way conductive circuit. Any sensed temperature may be detected at a terminal of the directional circuit connected to a control circuit that may be a known type.

Moreover, even if it so happens that a surge current attacks the two-way conductive directional circuit from a reverse direction to a biased direction thereof, one of the two one-way conductive circuits that is reversely biased can effectively conduct to let out the surge current that otherwise might damage a temperature sensing circuit.

According to an embodiment of the invention, the two-way conductive directional circuit comprises a pair of diode circuits having a first diode for sensing the temperature of the semiconductive element and a second diode for neutralizing an accumulated amount of electrostatic charges.

According to another species of the invention, the two-way conductive directional circuit comprises a pair of diode circuits either having a first diode formed with a forward direction thereof in accord with a one-way biased direction of the directional circuit, and a second diode formed with a forward direction thereof reverse to the one-way biased direction of the directional circuit.

According to the species of the invention, in an integrated semiconductor circuit, a directional circuit that is separated from a semiconductive element by an insulation film is adapted to sense a temperature of the semiconductor element, by providing a diode circuit thereof with a (temperature sensing) first diode having its forward direction directed in the direction of an easy flow of the directional circuit, and another diode circuit with a (charge neutralizing) second diode having its forward direction directed in the reverse direction to the direction of the easy flow of the directional circuit.

The first diode tends to conduct a current in the direction of easy flow of the directional circuit, whenever a forward

voltage is applied thereto, but the second diode does not. They are circuit components of the diode circuits of the directional circuit and may be connected in parallel to each other at non-defined terminals thereof: they may exemplarily be connected at a conductor joining or bonding area of a size-reduced chip. The directional circuit tends to conduct a current, substantially through the first diode, thus having a potential difference developed thereacross to be detected by a certain adapted circuit that may include a known control circuit for controlling the semiconductive element.

The detectable potential difference represents a voltage drop across the first diode that is proportional to a given temperature coefficient of the diode which itself may comprise a known polycrystalline silicon diode. The temperature coefficient of the first diode thus substitutes for that of the directional circuit, so that the value of the temperature coefficient is maintained as it is.

Moreover, to achieve the object, the present invention provides a method for operating an integrated semiconductor device including a semiconductive element and a two-way conductive directional circuit to be biased for sensing a temperature of the semiconductive element, the method comprising the steps of providing the directional circuit with a bias in either conductive direction thereof for sensing the temperature of the semiconductive element, and providing the directional circuit with a bias in the other conductive direction thereof for sensing the temperature of the semiconductive element.

According to the invention, a two-way conductive directional circuit which should have a pair of one-way conductive circuits is biased in either of two conductive directions thereof in a time-dividing manner. Either bias direction permits an effective temperature sensing of a semiconductive element and an effective cancellation of a charge accumulation tendency. Neither one-way conductive circuit is exclusively used for either the temperature sensing or the charge cancellation. That is, both are effectively utilized, permitting a relatively long service life to the device. Moreover, even if either one-way circuit is damaged, the other can substitute therefor. The time interval for switching the bias direction may be voluntarily set. It may equal to a unit time of an associated system clock or to substantially one half of an expected service life.

### BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention will become more apparent from the consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a cross sectional view of a conventional semiconductor device;

FIG. 2 is a circuit diagram showing an equivalent circuit of an essential part of the semiconductor device of FIG. 1;

FIG. 3 is a cross sectional view of a semiconductor device according to the invention;

FIG. 4A is a circuit diagram showing an equivalent circuit of an essential part of the semiconductor device of FIG. 3;

FIG. 4B is a circuit diagram showing a modified example of the essential part of FIG. 4A;

FIG. 5 is a graph showing a voltage vs. temperature relationship of a single diode for various forward currents having their associated temperature coefficients;

FIG. 6 is a graph showing a voltage vs. temperature relationship of a pair of reversely paralleled diodes for

various forward currents having their associated temperature coefficients; and

FIG. 7 is a circuit diagram showing another embodiment of the invention.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Description will be given of an integrated semiconductor circuit according to an embodiment of the invention, with reference to FIGS. 3 to 6. Like or corresponding parts to those of FIG. 1 are designated by like characters. Redundant description of some similar members are omitted for brevity.

FIG. 3 shows an enlarged transverse partial section of a semiconductor device according to an embodiment of the invention, and FIG. 4A shows an equivalent circuit of an essential individual part of the semiconductor device.

The semiconductor device includes a plurality of longitudinally arrayed N-channel depression type power MOS FETs 13 and a plurality of longitudinally arrayed two-way conductive directional circuits 20 in positions transversely one-to-one correspondent to the FETs 13. As shown in FIG. 4A, each two-way directional circuit 20 comprises a pair of one-way conductive circuits (a) and (b) each consisting of a diode 21 or 22 of a known type, respectively. The one-way conductive circuits (a) and (b) are electrically conductive in a reverse direction to each other, and are connected in parallel to each other at a conductor joining or bonding area of the semiconductor device.

The FETs are fabricated as follows:

First, an N<sup>+</sup> type silicon substrate 1 is fabricated in a well-known manner. Then, an N<sup>+</sup> type silicon epitaxial layer 2 is formed on the substrate 1, before forming a P type diffusion layer 8 as a depletion layer and an N type diffusion layer 5 in surface areas of the epitaxial layer 2.

After the formation of a lower layer (approx. 5000 Å thick) of an insulation film 10, a polycrystalline silicon layer 7 (approx. 6000 Å thick) is formed thereon as a gate layer, which is coated with an upper layer (approx. 500 Å thick) of the insulation film 10 and an interlayer insulation film 8 (approx. 5000 Å thick) formed thereon.

The directional circuits 20 are each provided in a layer-wise same position as the gate layer 7 of the FETs 13 by forming, in a separated manner therefrom, a polycrystalline silicon layer 23 (approx. 6000 Å thick) on the lower layer of the insulation film 10. The polycrystalline silicon layer 23 comprises a P type anode layer 24 and an N type cathode layer 25. On the silicon layer 23 also is formed an upper layer (approx. 500 Å thick) of the insulation film 10 and the interlayer insulation film 8 (approx. 5000 Å thick).

Each FET 13 is provided with a gate electrode 9a, a source electrode 9b and a drain electrode 12. Each diode 21, 22 has an anode electrode 26 and a cathode electrode 27, while they are shown in a combined form in the equivalent circuit of FIG. 4A.

It will be understood that in a plan view a plurality of local anode layer segments and a plurality of local cathode layer segments are longitudinally arrayed in a staggered and alternately intervening manner to constitute a longitudinal array of pairs of diodes 21, 22 put in a reverse parallel relation to each other, and each diode has the anode electrode 26 and the cathode electrode 27.

The individual part shown in FIG. 4A includes one FET 13 and one directional circuit 20 biased for sensing a peripheral temperature of the FET 13.

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The directional circuit 20 comprises the one-way conductive circuit (a) consisting of the diode 21 having its forward direction (i.e. the direction of an easy flow) in the direction from its anode electrode 26 to its cathode electrode 27 that is in accord with a biased direction of the directional circuit 20, which is subjected to a positive bias voltage  $V_f$  at a bias end terminal 28 thereof and is connected at a detection end terminal 29 thereof to an unshown FET control circuit of a known type; and the one-way conductive circuit (b) consisting of the diode 22 having its forward direction in the direction from the terminal 29 to the terminal 28 of the directional circuit, that is a reverse direction to the biased direction thereof. Accordingly, the circuit 20 is a two-way conductive directional circuit.

With the bias voltage  $V_f$  applied to the terminal 28 of the directional circuit 20, the forwardly biased diode 21 conducts a current  $I_f$  such that  $I_f = \Delta V / r_f$ , where  $\Delta V$  is a voltage drop across the diode 21, and  $r_f$  is an internal resistance of the diode 21 that varies depending upon the peripheral temperature of the FET 13.

However, the reversely biased diode 22 does not conduct any significant current, subject to a negligible or compensative leakage current, so that the voltage drop  $\Delta V$  across the diode 21 substantially substitutes for a total voltage drop across the circuit 20, which is detected at the detection end to provide a temperature signal to the FET control signal, where it is processed to turn off the FET 13 if the signal represents a critical temperature.

When undesirable positive and negative electrostatic charges tend to accumulate at both ends of the of the circuit 20 (i.e. at both sides of the cathode of each diode 21, 22), having an increasing electrostatic voltage developed thereacross to exert emfs on the charges, those charges tending to produce a current in the forward direction of the circuit 20 are neutralized through the forward biased diode 21 and the remaining charges tending to produce a current in the reverse direction to the forward direction of the circuit 20 are neutralized through the reverse biased diode 22.

Should a surge current happen to attack the directional circuit 20, the diodes 21, 22 cooperate with each other to let it out irrespective of the incoming direction of the surge current that otherwise might damage a one-way conductive diode circuit when it has occurred at a cathode end of the circuit.

FIG. 5 shows a number of voltage  $V_f$  vs. temperature curves of a temperature sensing single-diode circuit for various forward currents  $I_f$  (1 mA, 100  $\mu$ A, 10  $\mu$ A) having associated temperature coefficients  $\gamma_1$ , and FIG. 6 shows the same number of voltage  $V_f$  vs. temperature curves of the two-way conductive directional circuit 20 for equivalent forward currents  $I_f$  (1 mA, 100  $\mu$ A, 10  $\mu$ A) having associated temperature coefficients  $\gamma_2$ . Employed diodes are identical to each other in constitution and performance, except for the connection.

It will be seen from these Figures that the two-way conductive directional circuit 20 provides a competent temperature coefficient  $\gamma_2$  for each reference current.

Table 1 in the next page shows a comparison of the ESD durability between the circuit of FIG. 5 and the circuit of FIG. 6.

As will be seen from Table 1, the ESD durability is improved from 150 Vdc to 200 Vdc (i.e. approx. 33%) at the reverse bias end of circuit. This improvement is achieved by the provision of a reverse biased diode circuit (b) connected in parallel to a forward biased diode circuit (a).

According to the present embodiment of the invention, therefore, a two-way conductive directional circuit permits

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a competent temperature coefficient  $\gamma^{m/^\circ C}$  to be availed in addition to an improved ESD durability.

In this respect, the polycrystalline silicon layer or local region thereof may preferably have an adapted peripheral length to a yet improved ESD durability.

TABLE 1


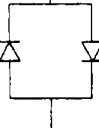
Connection	Durable voltage at forward end	Durable voltage at reverse end
	180 Vdc	150 Vdc
	200 Vdc	200 Vdc

FIG. 4B shows a modified example of the embodiment described. This Figure substantially corresponds to FIG. 4A, and like members to those of FIG. 4A are designated by like characters, without description. In this modification, a forward conductive diode circuit (a) of a two-way conductive directional circuit 20 comprises a plurality of forward biased diodes 21 connected in series, which gives an increased temperature coefficient.

It will be understood that a reverse conductive diode circuit (b) of the two-way conductive directional circuit 20 may also comprise a plurality of reverse biased diodes connected in series or parallel.

FIG. 7 shows an equivalent circuit of an essential part of an integrated semiconductor device according to another embodiment of the present invention. This Figure corresponds to FIG. 4A in constitution of an FET and a two-way conductive directional circuit, and like members to those of FIG. 4A are designated by like characters.

In this embodiment, a two-way conductive directional circuit 20 has a bias direction switching circuit 30 interconnected between the circuit 20 and an unshown external circuitry that includes a bias supply line, a temperature detecting FET control circuit and a clock signal supply line or a switching control circuit.

The switching circuit 30 comprises a cross switch for switching over the connection of a bias end terminal 28 of the directional circuit 20 from a bias supply side to a temperature detection side, and concurrently that of a detection end terminal 29 of the directional circuit 20 from the temperature detection side to the bias supply side, and vice versa. The cross switch is responsive to a clock signal or a switching control signal to effect the cross switching operation.

Through the switching circuit 30, the directional circuit 20 is operated so that it is provided with a bias in either conductive direction thereof for sensing a temperature of an associated FET 13 during a certain time interval, and with a bias in the other conductive direction thereof for sensing the temperature of the FET 13 during a subsequent time interval. The time intervals may be volutarily determined.

It will be seen that either bias direction permits an effective temperature sensing of the FET 13 as well as an

effective cancellation of a charge accumulation tendency, because the constitution of the directional circuit 20 is substantially symmetrical. Neither one-way conductive circuit (a) nor (b) is exclusively used for either the temperature sensing or the charge cancellation. That is, both (a) and (b) are effectively utilized, providing a relatively long service life of the device. Moreover, even if either circuit (a) or (b) is damaged, the other circuit (b) or (a) can substitute therefor.

While the present invention has been described with reference to the particular illustrative embodiments, it is not to be restricted by those embodiments but only by the appended claims. It is to be appreciated that those skilled in the art can change or modify the embodiments without departing from the scope and spirit of the present invention.

What is claimed is:

1. An integrated semiconductor device comprising:

a semiconductive element formed therein;

an insulation film formed on the semiconductive element;

a polycrystalline silicon layer formed on the insulation film;

a two-way conductive directional circuit formed in the silicon layer; and

the directional circuit being one-way biased for sensing a temperature of the semiconductive element.

2. The semiconductor device as claimed in claim 1, wherein:

the two-way conductive directional circuit comprises a pair of diode circuits, one of said diode circuits having a first diode for sensing the temperature of the semiconductive element and another of said diode circuits having a second diode for neutralizing an accumulated amount of electrostatic charges.

3. The semiconductor device as claimed in claim 1, wherein:

the two-way conductive directional circuit comprises a pair of diode circuits, one of said circuits having a first diode formed with a forward direction thereof in accord with a one-way biased direction of the directional circuit and another of said circuits having a second diode formed with a forward direction thereof reverse to the one-way biased direction of the directional circuit.

4. A method for operating an integrated semiconductor device including a semiconductive element and a two-way conductive directional circuit, the method comprising the steps of:

providing the directional circuit with a bias in one of two conductive directions thereof for sensing a temperature of the semiconductive element, and

providing the directional circuit with a bias in the other of the two conductive directions thereof for sensing the temperature of the semiconductive element.

\* \* \* \* \*



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**EXAMPLE:**

$$\begin{aligned}
 & (A + B + C')(A + B + D)(A + B + E)(A + D' + E)(A' + C) \\
 &= (A + B + C'D)(A + B + E)[AC + A'(D' + E)] \\
 &= (A + B + C'DE)(AC + A'D' + A'E) \\
 &= AC + \cancel{ABC} + A'BD' + A'BE + A'C'DE \quad (3-13)
 \end{aligned}$$

(What theorem was used to eliminate  $ABC$ ? Hint: let  $X = AC$ .)

In this example, if the ordinary distributive law (3-10) had been used to multiply out the expression by "brute force," 162 terms would have been generated and 158 of these terms would then have to be eliminated.

The same theorems that are useful for multiplying out expressions are useful for factoring. By repeatedly applying (3-10), (3-11), and (3-12) any expression can be converted to a product-of-sums form.

**EXAMPLE OF FACTORING:**

$$\begin{aligned}
 & AC + A'BD' + A'BE + A'C'DE \\
 &= \underbrace{AC}_{XZ} + \underbrace{A'(BD' + BE + C'DE)}_{X'Y} \\
 &= (A + BD' + BE + C'DE)(A' + C) \\
 &= [\underbrace{A + C'DE}_X + \underbrace{B(D' + E)}_{YZ}](A' + C) \\
 &= (A + B + C'DE)(A + C'DE + D' + E)(A' + C) \\
 &= (A + B + C')(A + B + D)(A + B + E)(A + D' + E)(A' + C) \quad (3-14)
 \end{aligned}$$

This is the same expression we started with in (3-13).

## 3.4 Exclusive-OR and Equivalence Operations

The *exclusive-OR* operation ( $\oplus$ ) is defined as follows:

$$\begin{aligned}
 0 \oplus 0 &= 0 & 0 \oplus 1 &= 1 \\
 1 \oplus 0 &= 1 & 1 \oplus 1 &= 0
 \end{aligned}$$

The truth table for  $X \oplus Y$  is

$X$	$Y$	$X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0



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(12) **United States Patent**  
Pages et al.

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(45) Date of Patent: **Apr. 16, 2002**

(54) **SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME**

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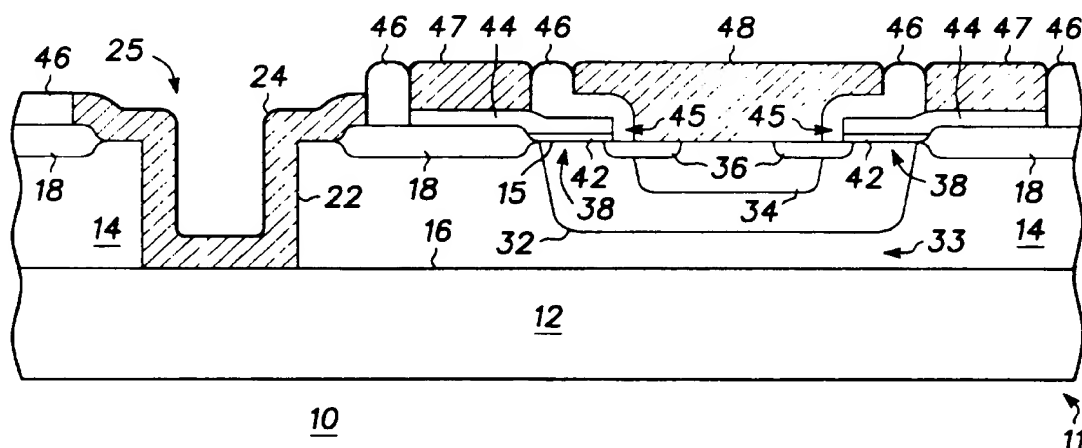
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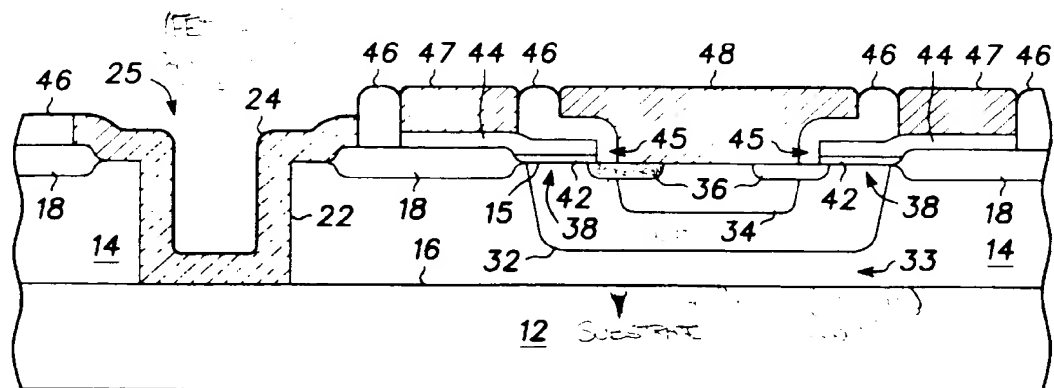
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(57) **ABSTRACT**

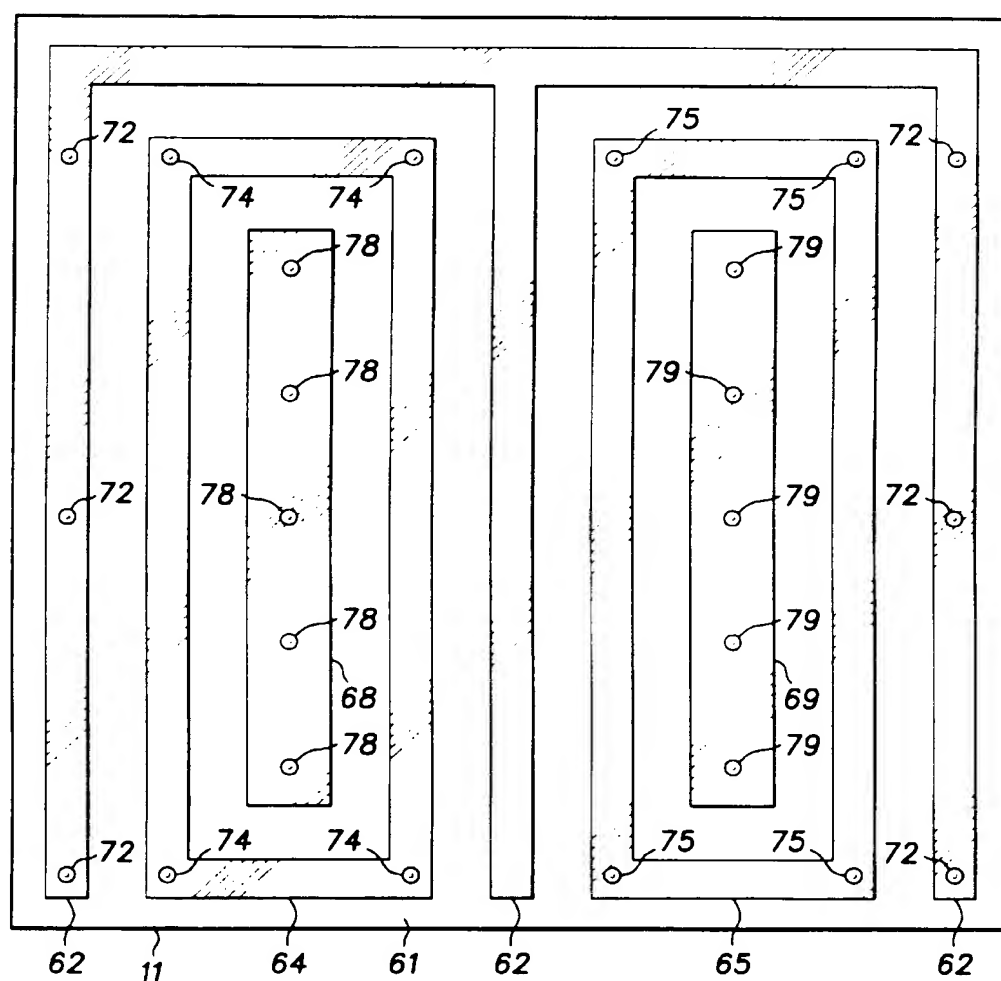
A vertically diffused FET (10) is fabricated on a semiconductor die (11) that includes an N<sup>+</sup> substrate (12) and an N<sup>+</sup> epitaxial layer (14). The FET (10) has a source region (36) and a channel region (38) near a front surface (15) of the epitaxial layer (14), and a drain region in the substrate (12). A trench (22) extends through the epitaxial layer (14) to the substrate (12). A conductive layer (24) fills the trench (22), thereby forming a conductive plug (25) electrically coupled to the substrate (12). The conductive plug (25) forms a top side drain electrode of the FET (10).

6 Claims, 1 Drawing Sheet





10 *FIG. 1*



60 *FIG. 2*

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## SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

### BACKGROUND OF THE INVENTION

The present invention relates, in general, to semiconductor devices and, more particularly, to vertical semiconductor devices.

Vertical semiconductor devices such as, for example, vertically diffused field effect transistors are commonly used as high power devices in electronic circuits. A conventional vertically diffused field effect transistor usually has its gate electrode and source electrode on the front side of a semiconductor die on which the transistor is fabricated. The drain electrode of the transistor is typically on the back side of the die. Inter-chip or inter-die wiring is conventionally used for coupling the drain electrode of the transistor to other elements in the circuit. The inter-chip wiring requires back side metal plating and wire bonding, which are complicated and expensive. As the complexity of the circuit increases, the number and complexity of the interconnections between different dies in the circuit also increase. Consequently, the inter-chip wiring process becomes increasingly expensive and increasingly difficult to perform.

Accordingly, it would be advantageous to have a vertical semiconductor device on a chip and a method for fabricating the device, so that the device can be coupled to an off-chip circuit element without wire-bonding to the back side of the chip. It is desirable for the device to be compatible with a simple and cost efficient packaging process. It is also desirable for the device and the interconnection between the device and other circuit elements in a circuit to be simple, reliable, and cost efficient. It would be of further advantage for the method for fabricating the device to be simple and compatible with existing semiconductor device fabricating processes.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a semiconductor device in accordance with the present invention; and

FIG. 2 is a schematic diagram of a flip-chip package that includes the semiconductor device of FIG. 1 in accordance with the present invention.

It should be understood that for simplicity and clarity of illustration, the figures are not necessarily drawn to scale. It should also be understood that, where considered appropriate, reference numerals have been repeated among the figures to indicate corresponding or analogous elements.

### DETAILED DESCRIPTION OF THE DRAWINGS

Generally, the present invention provides a semiconductor device and a method for fabricating the semiconductor device on a semiconductor die. More particularly, the device is a vertical semiconductor device that includes a conductive plug in the die. The conductive plug is electrically coupled to a region of the die near its back side. Therefore, an electrode of the vertical semiconductor device that would have been conventionally formed on the back side of the die is brought to the front side of the semiconductor die via the conductive plug. With all of its electrodes on the front side of the die, the vertical semiconductor device can be coupled to other elements of a circuit without wire bonding to the back side of the die.

A semiconductor device 10 in accordance with the present invention is schematically shown in FIG. 1. By way of example, semiconductor device 10 is a vertical field effect

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transistor (FET) and FIG. 1 shows a cross-sectional view of a portion of FET 10. Vertical FETs is often used in high power applications such as, for example, motor control, power supply switching, etc. For example, vertical FETs can be used as dual high side switches, H-Bridge switches, etc.

FET 10 is fabricated on a semiconductor die 11 that includes a body of a semiconductor material, i.e., a semiconductor substrate 12, and a semiconductor layer 14 over substrate 12. By way of example, semiconductor substrate 12 is a silicon substrate and semiconductor layer 14 is an epitaxially grown silicon layer. An active region of FET 10 is to be formed in epitaxial layer 14.

Substrate 12 is doped with ions of N conductivity type such as, for example, phosphorus ions or arsenic ions. Preferably, substrate 12 has a high dopant concentration, e.g., a dopant concentration between approximately  $1 \times 10^{17}$  atoms per cubic centimeter (atoms  $\text{cm}^{-3}$ ) and approximately  $1 \times 10^{21}$  atoms  $\text{cm}^{-3}$ , in order to achieve a high conductivity, i.e., a low resistivity. For example, the resistivity of substrate 12 is preferably lower than approximately 6 milliohm centimeters ( $\text{m}\Omega\text{-cm}$ ). Silicon doped with phosphorus ions at a very high dopant concentration, e.g., a dopant concentration greater than or equal to approximately  $5 \times 10^{20}$  atoms  $\text{cm}^{-3}$ , is sometimes referred to as red phosphorus silicon. Red phosphorus silicon has a very low resistivity, e.g., as low as approximately 1  $\text{m}\Omega\text{-cm}$ . Typically, red phosphorus silicon has a resistivity that is approximately 25% lower than that of a conventional N<sup>+</sup> doped silicon. Therefore, red phosphorus silicon is a preferred material for substrate 12 in order to achieve a small series resistance of FET 10. The series resistance of FET 10 also depends on the thickness of substrate 12. By way of example, the thickness of substrate 12 is in a range between approximately 200 micrometers ( $\mu\text{m}$ ) and approximately 800  $\mu\text{m}$ .

Epitaxial layer 14 is also doped with ions of N conductivity type such as, for example, phosphorus ions or arsenic ions. The dopant concentration of epitaxial layer 14 is lower than that of substrate 12. That is, epitaxial layer 14 is lightly doped with N conductivity type ions. For example, the dopant concentration of epitaxial layer 14 is in a range between approximately  $1 \times 10^{16}$  atoms  $\text{cm}^{-3}$  and approximately  $1 \times 10^{18}$  atoms  $\text{cm}^{-3}$ , and epitaxial layer 14 has a thickness between approximately 1  $\mu\text{m}$  and approximately 5  $\mu\text{m}$ . The breakdown voltage of FET 10 depends on the dopant concentration and thickness of epitaxial layer 14. For example, the thickness of epitaxial layer 14 is preferably in a range between approximately 3  $\mu\text{m}$  and approximately 4  $\mu\text{m}$  if FET 10 is designed to have a breakdown voltage of approximately 30 volts (V). Epitaxial layer 14 has a major surface 15 opposite to an interface 16 between substrate 12 and epitaxial layer 14. Major surface 15 is also referred as a front surface of epitaxial layer 14.

Field oxide regions 18 are disposed over portions of major surface 15 in a local oxidation of silicon (LOCOS) process. Field oxide regions 18 serve as isolation structures that provide isolation between different electrodes of FET 10. An ion implantation is optionally performed before forming field oxide regions 18 to form heavily doped regions (not shown) under field oxide regions 18. The heavily doped regions (not shown) prevent inadvertent turning on of parasitic field effect transistors formed under field oxide regions 18. It should be understood that the isolation structures on epitaxial layer 14 can be formed using other processes such as, for example, poly-bullered LOCOS, poly-encapsulated LOCOS, etc.

Epitaxial layer 14 has a trench 22 formed therein. Trench 22 extends from major surface 15 through epitaxial layer 14

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to interface 16. Alternatively, trench 22 extends partially into substrate 12. In other words, the bottom of trench 22 is either on interface 16 or inside substrate 12. By way of example, trench 22 is formed via an anisotropic etching process. A conductive layer 24 fills trench 22. Suitable materials for conductive layer 24 include aluminum and its alloys, such as, for example, aluminum-silicon alloy, aluminum-silicon-copper alloy, aluminum-copper alloy, aluminum-tungsten alloy, and the likes. So, conductive layer 24 is sometimes also referred to as a metal layer. Techniques for forming conductive layer 24 in trench 22 include chemical vapor deposition, sputtering, etc. FIG. 1 shows that conductive layer 24 is formed on the bottom and the sidewall of trench 22. It should be noted that this is not intended as a limitation of the present invention. In an alternative embodiment, the conductive material completely fills trench 22. Conductive layer 24 and trench 22 form a conductive plug 25 extending from major surface 15 through epitaxial layer 14 and in contact with substrate 12.

Ions of P conductivity type such as, for example, boron ions are doped into a portion of epitaxial layer 14 to form a P conductivity type well 32 that extends from major surface 15 into epitaxial layer 14. Well 32 serves as an active region of FET 10. In one embodiment, well 32 extends partially into epitaxial layer 14, i.e., well 32 has a depth less than the thickness of epitaxial layer 14. Therefore, there is a region 33 between well 32 and substrate 12 that remains as lightly doped with N conductivity type ions. In an alternative embodiment (not shown), well 32 extends all the way through epitaxial layer 14 to interface 16, i.e., well 32 has a depth substantially equal to the thickness of epitaxial layer 14. Well 32 can be formed in an ion implantation process, a diffusion process, or a combination thereof. In a preferred embodiment, the depth of well 32 is between approximately 0.8  $\mu\text{m}$  and approximately 1.8  $\mu\text{m}$ . When FET 10 is designed to have a breakdown voltage of approximately 30 V, the thickness of well 32 is preferably between approximately 1  $\mu\text{m}$  and approximately 1.5  $\mu\text{m}$ . The dopant concentration of well 32 is preferably between approximately  $1 \times 10^{16}$  atoms/ $\text{cm}^3$  and approximately  $1 \times 10^{18}$  atoms/ $\text{cm}^3$ . Because of its relatively low dopant concentration, well 32 is also referred to as a P<sup>+</sup> well.

A P<sup>+</sup> doped region 34 is formed within well 32 by doping additional P conductivity type ions into a portion of P<sup>+</sup> well 32 adjacent major surface 15. The dopant concentration of P<sup>+</sup> doped region 34 is preferably between approximately  $1 \times 10^{17}$  atoms/ $\text{cm}^3$  and approximately  $1 \times 10^{20}$  atoms/ $\text{cm}^3$ . P<sup>+</sup> doped region 34 has a depth less than that of well 32. For example, the depth of P<sup>+</sup> doped region 34 ranges between approximately 0.25  $\mu\text{m}$  and approximately 1  $\mu\text{m}$ . A more preferred range for the depth of P<sup>+</sup> doped region 34 is between approximately 0.4  $\mu\text{m}$  and approximately 0.6  $\mu\text{m}$ . Like well 32, P<sup>+</sup> doped region 34 can be formed in an ion implantation process, a diffusion process, or a combination thereof. In operation, P<sup>+</sup> doped region 34 functions as a body contact region of FET 10.

Ions of N conductivity type such as, for example, arsenic ions or phosphorus ions are doped into a portion of well 32 to form an N<sup>+</sup> doped region 36 adjacent major surface 15. Preferably, N<sup>+</sup> doped region 36 is formed as a ring in well 32, and FIG. 1 shows a cross section of the ring structure. The dopant concentration of N<sup>+</sup> doped region 36 is preferably between approximately  $1 \times 10^{19}$  atoms/ $\text{cm}^3$  and approximately  $1 \times 10^{21}$  atoms/ $\text{cm}^3$ . N<sup>+</sup> doped region 36 has a depth less than that of well 32. For example, the depth of N<sup>+</sup> doped region 36 ranges between approximately 0.25  $\mu\text{m}$  and approximately 1  $\mu\text{m}$ . A more preferred range for the depth of

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N<sup>+</sup> doped region 36 is between approximately 0.4  $\mu\text{m}$  and approximately 0.6  $\mu\text{m}$ . Like well 32, N<sup>+</sup> doped region 36 can be formed in an ion implantation process, a diffusion process, or a combination thereof. In operation, N<sup>+</sup> doped region 36 functions as a source region of FET 10.

A dielectric layer 42 is disposed over major surface 15 of epitaxial layer 14. By way of example, dielectric layer 42 is a layer of silicon dioxide and has a thickness between approximately 30 nanometers (nm) and approximately 80 nm. Dielectric layer 42 can be disposed on major surface 15 via an oxidation process, a deposition process, or the like. A conductive layer such as, for example, a polycrystalline silicon layer 44 is disposed over dielectric layer 42. In a preferred embodiment, a portion of polysilicon layer 44 overlying well 32 has a thickness between approximately 400 nm and approximately 700 nm. Polysilicon layer 44 is preferably doped to increase its conductivity. Polysilicon layer 44 and dielectric layer 42 are patterned to overlie a portion of well 32 that is adjacent source region 36. After patterning, portions of polysilicon layer 44 and dielectric layer 42 overlying well 32 function as a gate structure 45 of FET 10. The portion of well 32 underlying gate structure 45 functions as a channel region 38 of FET 10.

A dielectric separation layer 46 is disposed over gate structure 45 and over portions of major surface 15 adjacent gate structure 45. Dielectric separation layer 46 forms spacers around gate structure 45. In a preferred embodiment, dielectric separation layer 46 is made of trimethyl phosphite doped tetraethyl orthosilicate. It should be noted that dielectric separation layer 46 can also be formed from other insulating materials such as silicon nitride, silicon dioxide, or the like.

Conductive structures 47 and 48 are disposed over epitaxial layer 14. Conductive structures 47 and 48 are separated from each other by dielectric separation layer 46. Conductive structure 47 is in contact with polysilicon layer 44 and functions as a gate electrode of FET 10. Preferably, conductive structure 47 is formed as a ring over polysilicon layer 44, and FIG. 1 shows a cross section of the ring structure. Conductive structure 48 overlies and is in contact with source region 36 and body contact region 34. Conductive structure 48 functions as a source electrode of FET 10. Like conductive layer 24 in trench 22, gate electrode 47 and source electrode 48 can be formed from any conductive material such as, for example, aluminum, aluminum-silicon alloy, aluminum-silicon-copper alloy, aluminum-copper alloy, aluminum-tungsten alloy, etc. Techniques for forming gate electrode 47 and source electrode 48 include chemical vapor deposition, sputtering, etc. Further, the formation of gate electrode 47 and source electrode 48 can be performed simultaneously with the process of forming conductive layer 24 in trench 22.

FIG. 1 shows source electrode 48 in contact with both source region 36 and body contact region 34. Therefore, FET 10 is a three-terminal device with its source bias and body bias coupled together. It should be noted that this is not a limitation of the present invention. In an alternative embodiment, source electrode 48 is in contact only with source region 36, and another conductive structure (not shown) is formed over epitaxial layer 14 and is in contact with body contact region 34. In such alternative embodiment, FET 10 is a four-terminal device.

After forming conductive structures 47 and 48, a dielectric layer (not shown in FIG. 1) is formed over epitaxial layer 14 and serving as an interlayer dielectric (ILD). Using techniques well known in the art, metallization regions (not

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shown in FIG. 1) are formed in the ILD to lead the electrodes of FET 10 to the upper surface of the ILD. It should be understood that the ILD and the metallization regions therein are optional in FET 10.

In FET 10, substrate 12 functions as a drain region. In operation, FET 10 conducts an electric current when charge carriers, i.e., electrons, flow from source region 36, through well 32, and into substrate 12. After reaching substrate 12, charge carriers flow out of die 11 via conductive plug 25. Therefore, conductive plug 25 functions as a drain electrode of FET 10. Because it leads charge carriers away from FET 10 through the top side of die 11, conductive plug 25 is also referred to as a top side drain electrode or an up-drain electrode of FET 10. Trench 22 is also referred to as a top side drain trench or an up-drain trench.

N<sup>+</sup> doped region 33 in epitaxial layer 14 between P<sup>+</sup> well 32 and substrate 12 functions as a lightly doped drain extension region (LDD) of FET 10. LDD 33 can effectively increase the break down voltage of FET 10. In accordance with the present invention, P<sup>+</sup> well 32 can be as deep as the thickness of epitaxial layer 14. In other words, LDD 33 is an optional feature in FET 10.

It should be noted that FIG. 1 is a cross-sectional view of only a portion of FET 10. Like many conventional power devices, FET 10 preferably has a multi-finger structure. In other words, FET 10 preferably includes a plurality of P<sup>+</sup> wells formed in epitaxial layer 14, each P<sup>+</sup> well having a structure similar to that of well 32. In each of the P<sup>+</sup> wells formed in epitaxial layer 14, there is a P<sup>+</sup> body contact region like P<sup>+</sup> body contact region 34, a source region like source region 36, and a channel region like channel region 38. FET 10 also preferably includes a plurality of source electrodes formed over epitaxial layer 14, each source electrode, e.g., source electrode 48, overlies a respective P<sup>+</sup> well, e.g., well 32, and is in contact with a respective source region, e.g., source region 36, and a respective P<sup>+</sup> body contact region, e.g., body contact region 34. A plurality of gate structures overlie the channel regions in the P<sup>+</sup> wells. Each gate structure, e.g., gate structure 45, includes a dielectric layer, e.g., dielectric layer 42, and a conductive layer, e.g., polysilicon layer 44, and overlies a respective channel region, e.g., channel region 38, in a respective P<sup>+</sup> well, e.g., P<sup>+</sup> well 32. In addition, conductive plug 25 preferably has a multi-finger structure, of which FIG. 1 shows the cross section of only one finger. Each finger of conductive plug 25 is preferably disposed adjacent to a corresponding P<sup>+</sup> well.

Because FET 10 has all its electrodes at the front side of die 11, the packaging of FET 10 is simple and easy. In addition, FET 10 can be coupled to other circuit elements (not shown) without wire bonding to the back side of semiconductor die 11. Although FET 10 is described hereinbefore as a vertical n-channel insulated gate FET, it should be understood that this is not a limitation of the present invention. The principle of the present invention can be practiced in the fabrication of any kind of vertical semiconductor device such as, for example, a vertically diffused p-channel insulated gate FET, a vertical bipolar transistor, a vertical metal semiconductor field effect transistor (MESFET), a vertical resistor, a capacitor, etc. When forming a resistor, the whole epitaxial layer may serve as an active region of the resistor.

FIG. 2 is a schematic diagram of a flip-chip package 60 that includes FET 10 formed on semiconductor die 11 as shown in FIG. 1 in accordance with the present invention. More particularly, FIG. 2 illustrates a front view of flip-chip package 60. By way of example, semiconductor die 11 has

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two P<sup>+</sup> wells like well 32 shown in FIG. 1, and trench 22 of FIG. 1 has a three-finger structure. A passivation layer (not shown) is usually disposed on the back side of die 11. The passivation layer protects the back side of substrate 12.

In one embodiment (shown in FIG. 2), the front side of die 11 is covered with an ILD 61. Conductive structures, e.g., metallization regions 62, 64, 65, 68, and 69 are formed in ILD 61. Metallization region 62 overlies and is electrically coupled to conductive plug 25 of FIG. 1. Metallization regions 64 and 65 overlie and are electrically coupled to corresponding conductive structures that form the gate electrodes of FET 10, e.g., gate electrode 47 shown in FIG. 1. Metallization regions 68 and 69 overlie and are electrically coupled to corresponding conductive structures that form the source electrodes of FET 10, e.g., source electrode 48 shown in FIG. 1. The front side of die 11 is then planarized. Conductive bumps 72 are formed on metallization region 62 and serve as a drain electrode of FET 10 in flip-chip package 60. Conductive bumps 74 are formed on metallization region 64, and conductive bumps 75 are formed on metallization region 65. Conductive bumps 74 and 75 serve as a gate electrode of FET 10 in flip-chip package 60. Conductive bumps 78 are formed on metallization region 68, and conductive bumps 79 are formed on metallization region 69. Conductive bumps 78 and 79 serve as a source electrode of FET 10 in flip-chip package 60. Conductive bumps 72, 74, 75, 78, and 79 can be formed from any conductive material such as, for example, copper, aluminum, silver, tungsten, gold, etc. via conventional means. It should be noted that the numbers of conductive bumps 72, 74, 75, 78, and 79 are not limited to that shown in FIG. 2. In accordance with the present invention, the number of conductive bumps formed on each of conductive structures 62, 64, 65, 68, and 69 can be any number greater than or equal to one.

In an alternative embodiment (not shown in FIG. 2) of the present invention, dielectric separation layer 46 (shown in FIG. 1), and the conductive structures that form top side drain electrode 25 (shown in FIG. 1), gate electrode 47 (shown in FIG. 1), and source electrode 48 (shown in FIG. 1) are exposed at the front side of semiconductor die 11. Conductive bumps are formed directly on the conductive structures after the front side of die 11 is planarized. The conductive bumps serve as the drain, gate, and source electrodes of FET 10.

It should be understood that the structure of FET 10 is not limited to being that described hereinbefore. For example, FET 10 is not limited to having two P<sup>+</sup> wells as shown in FIG. 2. FET 10 can have any number of P<sup>+</sup> wells, e.g., one, three, four, five, six, etc. Further, top side drain electrode 62 is not limited to having a three-finger structure as shown in FIG. 2. FET 10 can also include a plurality of multi-finger elements coupled together. Each multi-finger element has a structure similar to that described hereinbefore and shown in FIG. 2.

Flip-chip package 60 can be mounted on a circuit board (not shown) and coupled to other circuit elements (not shown) using techniques well known in the art. When FET 10 is a power device, a heat sink (not shown) can be attached to the back side of die 11 to alleviate the temperature of FET 10. The connection between FET 10 and other circuit elements is achieved through conductive bumps 72, 74, 75, 78, and 79. There is no wire-bonding to the back side of die 11.

By now it should be appreciated that a vertical semiconductor device and a method for fabricating the device on a semiconductor die have been provided. The vertical semi-

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conductor device of the present invention includes a conductive plug in the semiconductor die. The conductive plug is in contact with a region of the die near its back side. Therefore, an electrode of the device that would have been conventionally formed on the back side of the die is brought to the front side of the die via the conductive plug. With all of its electrodes on the front side of the die, the device can be coupled to other elements of a circuit without wire bonding to the back side of the die. The device fabricated in accordance with the present invention can be packaged in a flip-chip package and mounted on a circuit board. The fabrication of the device in accordance with the present invention is simple and compatible with existing semiconductor device fabricating processes. The process of interconnecting the device to other circuit elements using the flip-chip packaging techniques is simple, reliable, and cost efficient.

What is claimed is:

1. A field effect transistor, comprising:

- a body of semiconductor material of a first conductivity type and a first dopant concentration;
- a layer of semiconductor material epitaxial grown over said body, said layer having a major surface and a thickness, and being of the first conductivity type and a second dopant concentration that is lower than the first dopant concentration;
- a well having a first depth and of a second conductivity type and a third dopant concentration in said layer adjacent the major surface;
- a first doped region having a second depth less than the first depth and of the first conductivity type in said well adjacent the major surface of said layer;
- a gate structure over the major surface of said layer and patterned to overlie a portion of said well adjacent said first doped region; and

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a conductive plug extending through said layer and electrically coupled to said body, wherein a conductive path is formed through the body of semiconductor material between the conductive plug and a first conductive structure.

2. The field effect transistor of claim 1, wherein the first depth is less than the thickness of said layer.

3. The field effect transistor of claim 1, further comprising a second doped region of the second conductivity type and a fourth dopant concentration in said well adjacent said first doped region, the fourth dopant concentration being higher than the third dopant concentration.

4. The field effect transistor of claim 1, wherein said conductive plug includes

- a trench through said layer; and
- a metal layer in said trench.

5. The field effect transistor of claim 1, further comprising:

- a first conductive structure over the major surface of said layer and electrically coupled to said first doped region;
- a second conductive structure over the major surface of said layer and electrically coupled to said gate structure; and
- a third conductive structure over the major surface of said layer and electrically coupled to said conductive plug.

6. The field effect transistor of claim 5, further comprising:

- a first conductive bump electrically coupled to said first conductive structure;
- a second conductive bump electrically coupled to said second conductive structure; and
- a third conductive bump electrically coupled to said third conductive structure.

\* \* \* \* \*





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## United States Patent [19]

Yabusaki et al.

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[45] Date of Patent: Apr. 21, 1992

## [54] NUCLEAR MAGNETIC RESONANCE IMAGING APPARATUS

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[73] Assignees: Hitac Hi, Ltd.; Hitachi Medical Corporation, both of Tokyo, Japan

[21] Appl. No.: 473,428

[22] Filed: Feb. 1, 1990

## [30] Foreign Application Priority Data

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[51] Int. Cl.<sup>5</sup> ..... G01R 33/20

[52] U.S. Cl. .... 324/318; 324/322

[58] Field of Search ..... 324/318, 322, 307, 309, 324/320; 128/653 SC

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Primary Examiner—Hezron E. Williams

Assistant Examiner—Louis M. Arana

Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus

[57]

## ABSTRACT

In an imaging apparatus using the nuclear magnetic resonance, a solenoid coil and a slot-resonator coil are combined with each other so as to constitute a quadrature-phase detection probe. In order to operate the slot-resonator coil at low frequency, inductance is added to the slot-resonator coil. Further in order to cut the coupling between a transmitting coil and a receiving coil in a cross coil system, a capacitor together with the added inductance to form a resonant circuit is connected in parallel to the inductance. A favorable probe can be obtained in a vertical-magnetic field type imaging apparatus.

11 Claims, 11 Drawing Sheets

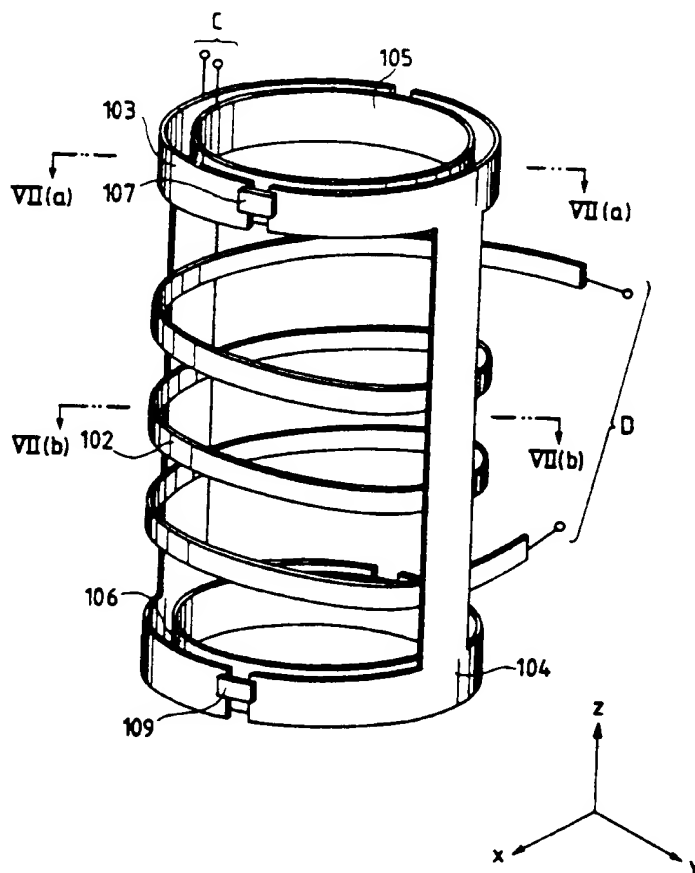


FIG. 2

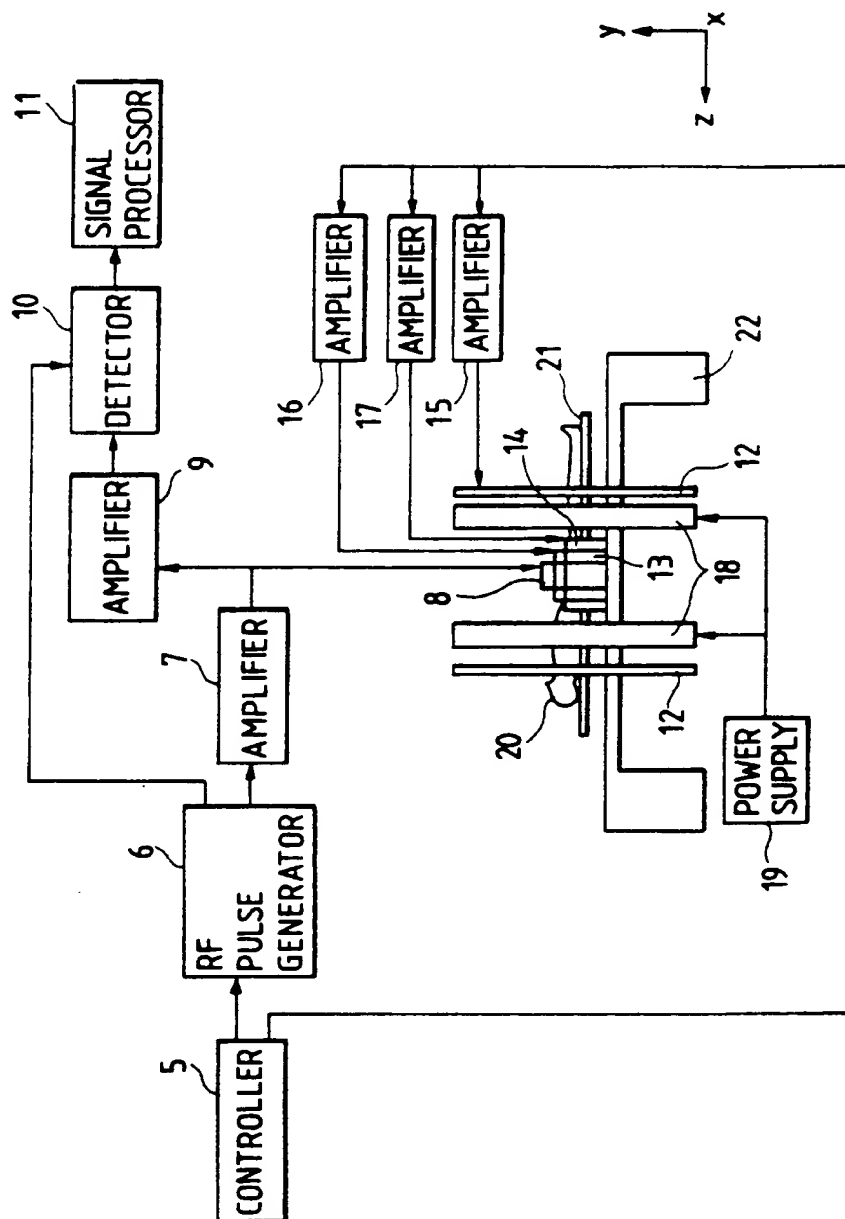


FIG. 3

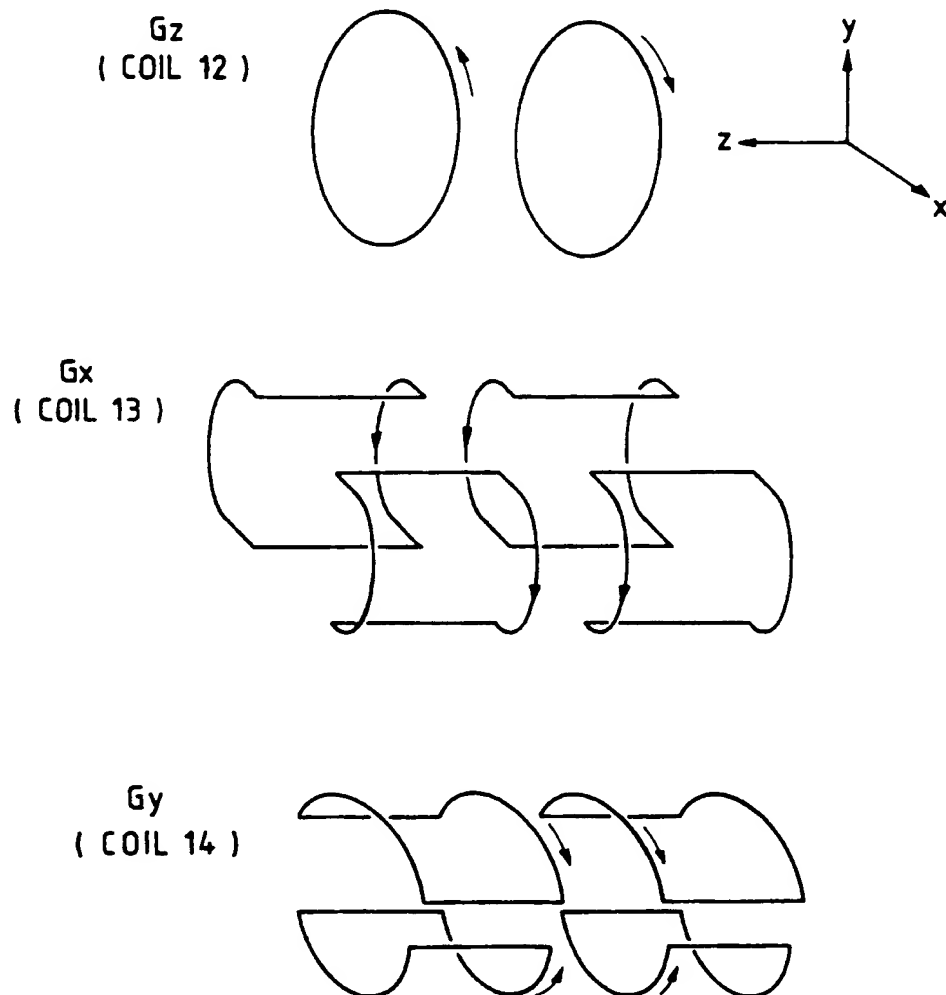


FIG. 4

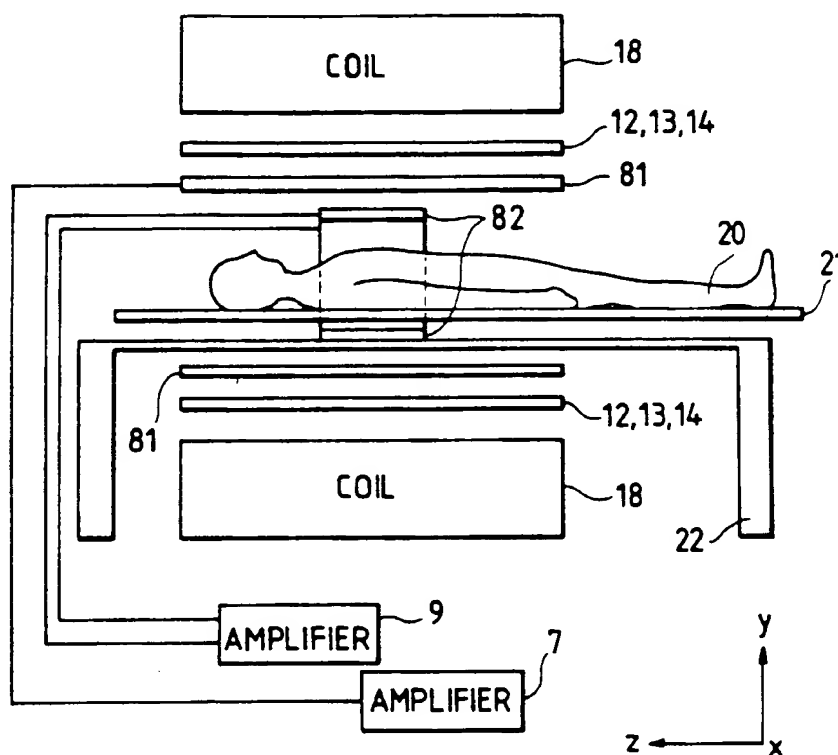


FIG. 6(a)

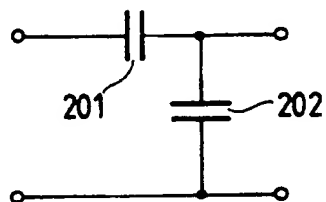


FIG. 6(b)

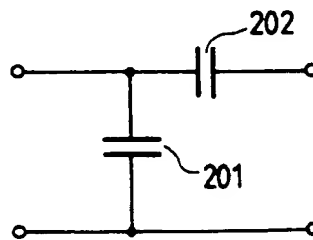


FIG. 5

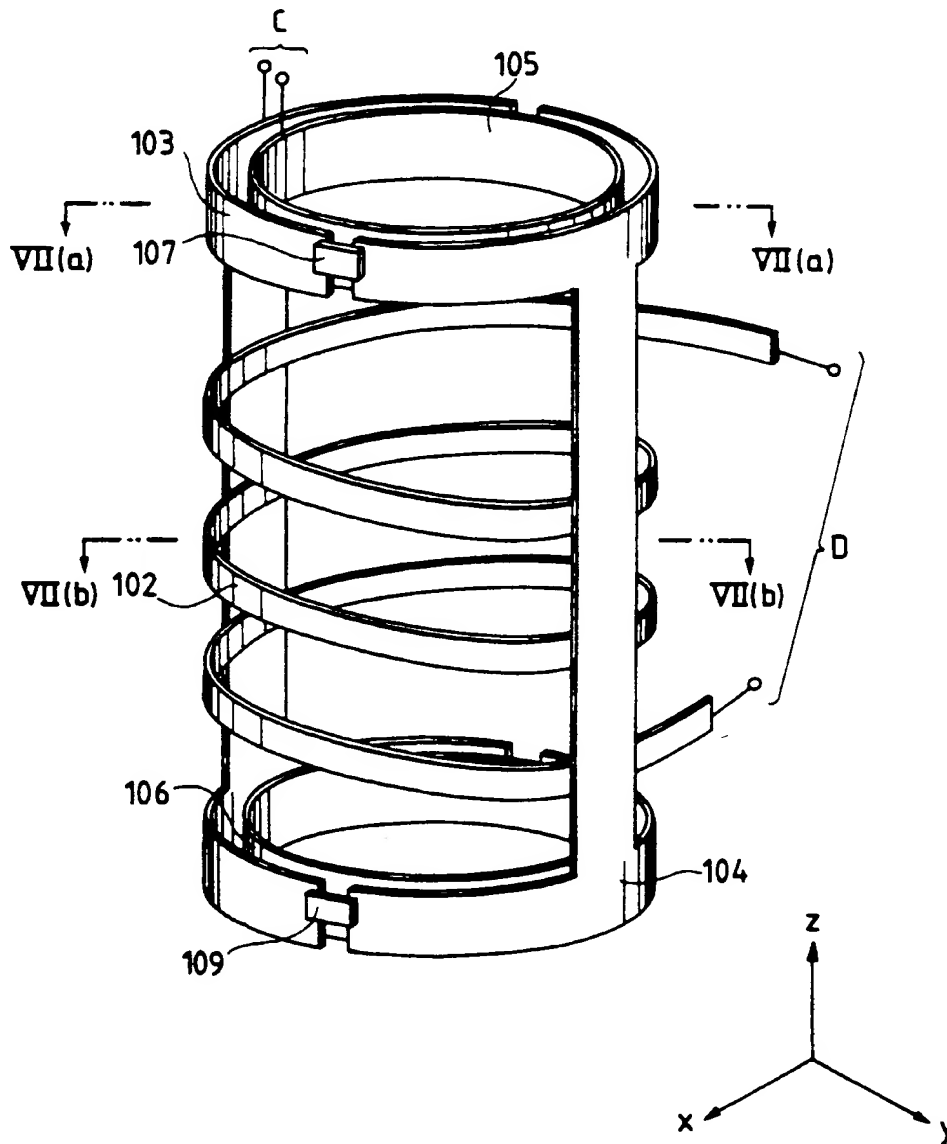


FIG. 7(a)

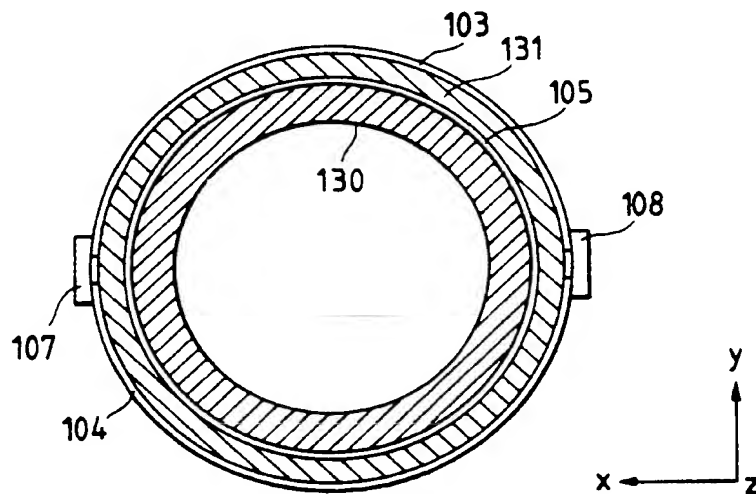


FIG. 7(b)

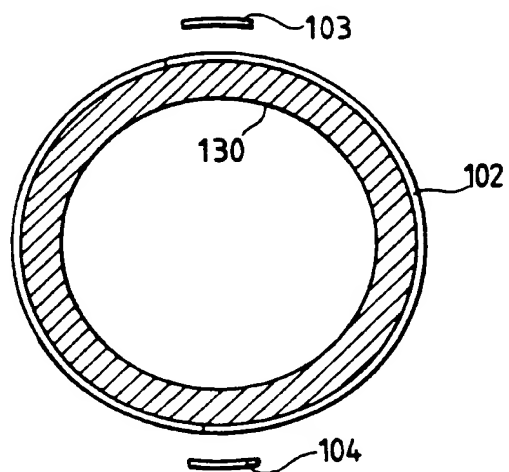


FIG. 8

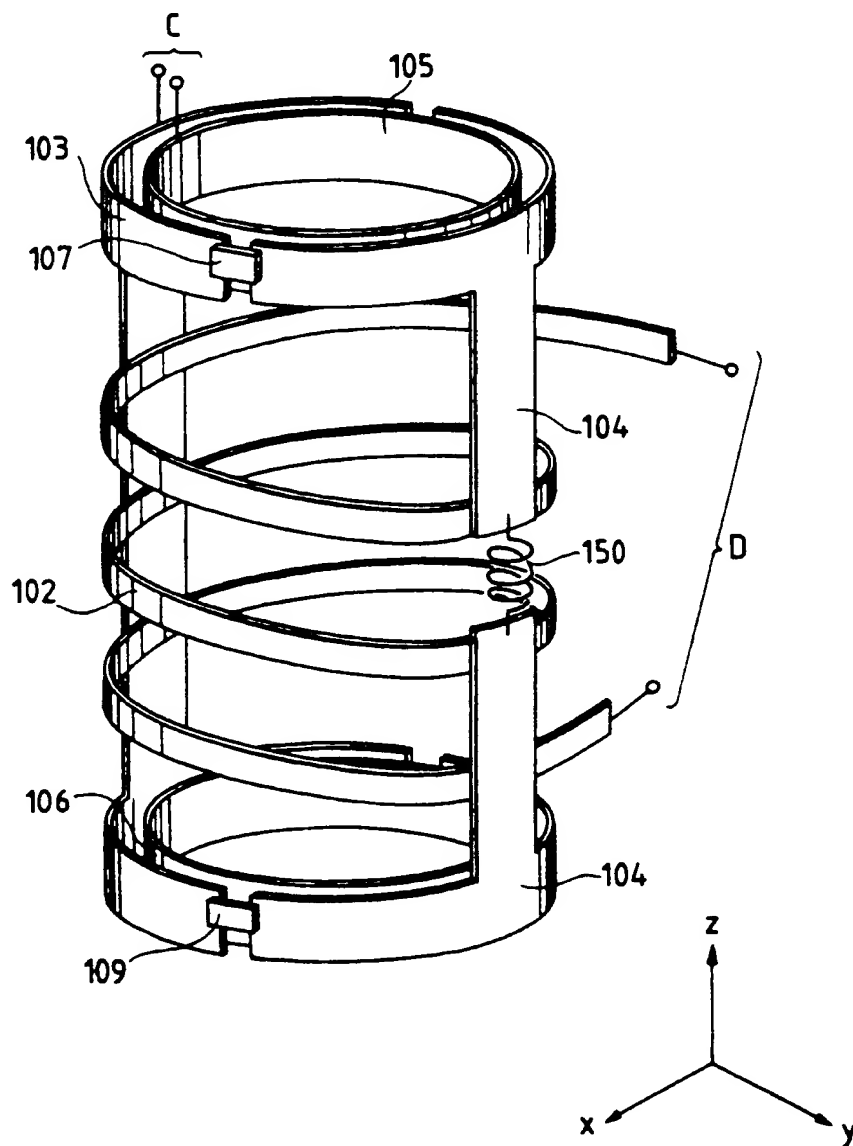


FIG. 9

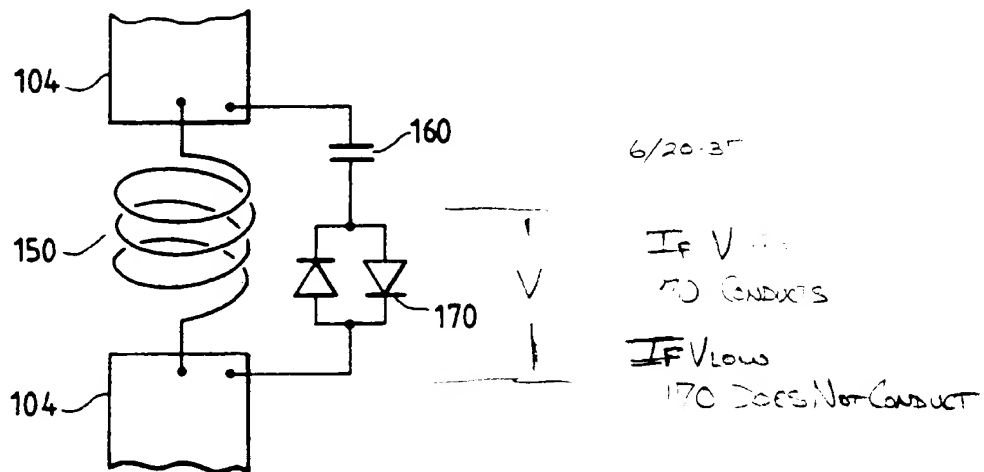


FIG. 10

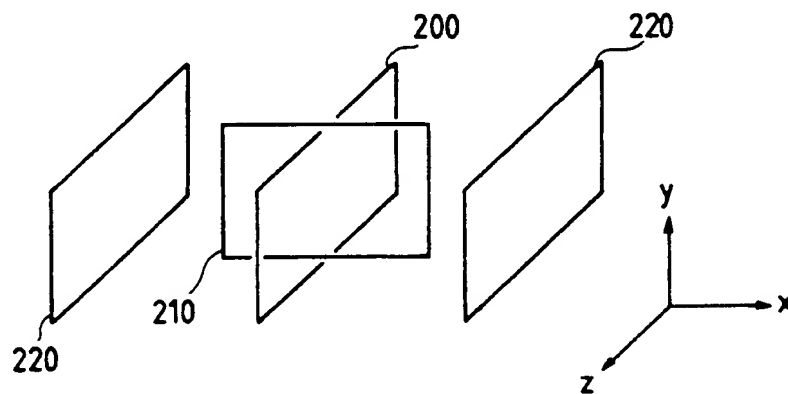




FIG. 11

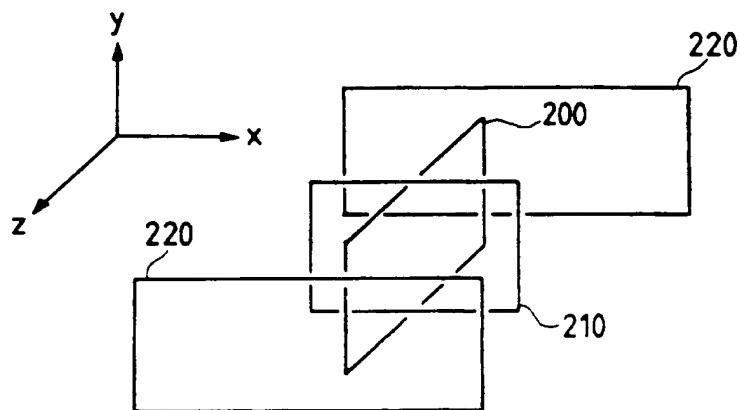


FIG. 12

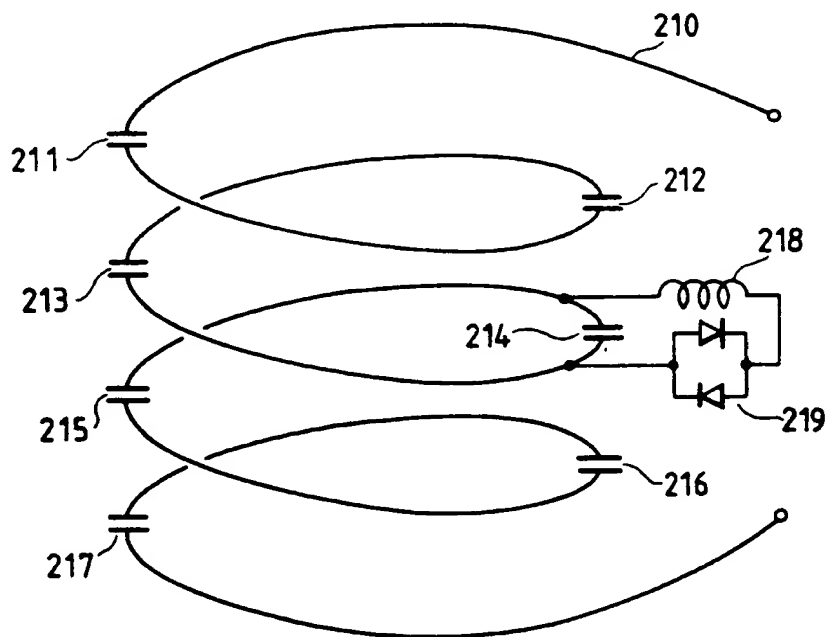
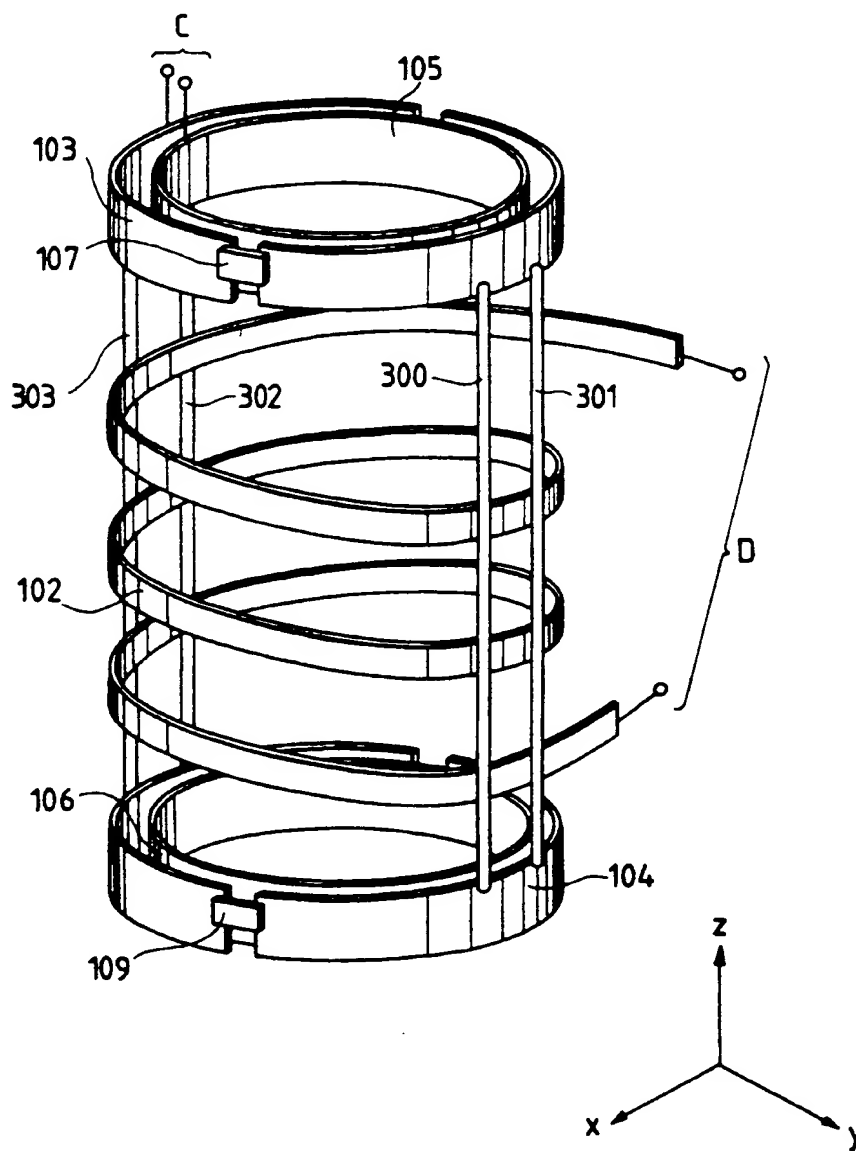


FIG. 13





# NUCLEAR MAGNETIC RESONANCE IMAGING APPARATUS

## BACKGROUND OF THE INVENTION

The present invention relates to an imaging apparatus using the nuclear magnetic resonance where a quadrature-phase detecting probe constituted by combination of a solenoid coil and a slot-resonator coil is used as a signal detection device.

In the prior art, an X-ray CT and an ultrasonic imaging apparatus have been used as an apparatus for the nondestructive inspection of an internal structure such as of a human brain and abdomen. In recent years, trial to image the internal structure of an object using a nuclear magnetic resonance (hereinafter abbreviated as "NMR") phenomenon succeeds thereby many sorts of information can be obtained although not obtained by an X-ray CT or an ultrasonic imaging apparatus. In an imaging apparatus using the NMR phenomenon, a signal from an object to be inspected must be separated and discriminated for each position of the object to be inspected. As one such method, a gradient magnetic field is applied to an object to be inspected thereby the magnetic field intensity in each position of the object is made different hence a resonant frequency or a phase encoding value in each position is made different so as to obtain information of the position.

## DESCRIPTION OF THE PRIOR ART

The basic principle of this method is described in detail in "Journal of Magnetic Resonance", vol. 18, pp. 69-83 or "Physics in Medicine & Biology", vol. 25, pp. 751-756.

In the imaging as above described, improvement of the efficiency of the probe coil for generating or receiving a high-frequency magnetic field becomes the important problem leading to improvement of the picture quality and decrease of the image pick-up time. As one means to solve the problem, a quadrature-phase detection probe coil (hereinafter abbreviated as a "QD probe") is described in "Journal of Magnetic Resonance", vol. 69 (1987), pp. 236-242.

The prior art as above described is effective as a QD probe in a horizontal-magnetic field type imaging apparatus using NMR (hereinafter abbreviated as a "horizontal-magnetic field type MRI apparatus"). A bird's eye view of a QD probe in the prior art is shown in FIG. 1. The QD probe in the prior art is constituted by two sets of guard rings 105, 106, and signal electrodes 111, 112, 113, 114 opposed to the guard rings 105, 106 through an insulator such as polytetrafluorethylene (omitted in FIG. 1), and has a structure such that capacitors 115 - 118, 119 - 122 are connected between respective signal electrodes. This may be considered to be a structure such that a first slot-resonator coil constituted by the signal electrodes 111, 113 and the two guard rings and a second slot resonator constituted by the signal electrodes 112, 114 and the two guard rings are combined in the perpendicular direction.

In the QD probe shown in FIG. 1, signals from feeding points A, B are added after the phase difference between them is compensated thereby the QD probe has sensitivity in the direction within the xy plane. In this case, from the principle of the nuclear magnetic resonance, the direction of the magnetic field is the z axis direction. Also the human body inserting direction is assumed to be the z-axis direction. Since the cylinder

center axis of the probe and the human body inserting direction are coincident, the human body shape and the probe shape are coincident. Consequently the signal detection efficiency is improved.

## SUMMARY OF THE INVENTION

If the probe in this state is applied to a vertical-magnetic field type imaging apparatus using NMR (hereinafter abbreviated as a "vertical-magnetic field type MRI apparatus"), the human body must be inserted between portions of the signal electrode in parallel to the cylindrical axis (hereinafter referred to as "vertical electrodes"). Consequently, the signal detection efficiency is lowered and the adoption of the QD probe becomes meaningless. That is, the QD probe shown in FIG. 1 cannot be applied to the vertical-magnetic field type MRI apparatus.

An object of the invention is to provide a QD probe which can be applied to a vertical-magnetic field type MRI apparatus.

In order to attain the foregoing object, according to the invention, a solenoid coil and a slot-resonator coil are combined so as to constitute a QD probe.

Also since the slot-resonator coil is operated at low frequency, inductance is added to an arm section of the slot-resonator coil.

Further, in order to decouple a transmitting coil and a receiving coil in a cross coil system, together with the added inductance, a capacitor resonated in the resonant frequency of the slot-resonator coil is connected in parallel to the added inductance. Also a switch is installed so that the operation of the resonant circuit constituted by the added inductance and the capacitance can be controlled at the transmitting state and the receiving state. The switch acts so that the resonant circuit resonates at the transmitting state and does not resonate at the receiving state. As a result, the coupling between the transmitting coil and the receiving coil at the transmitting state can be cut.

The switch is constituted by paired diodes, thereby the resonant circuit is controlled so that it resonates at the transmitting state and does not resonate at the receiving state.

Also the arm section of the slot-resonator coil is constituted by a slender conductor such as a copper pipe and the like, thereby overlapping between the slot-resonator coil and the solenoid coil is made as small as possible. Consequently, coupling between both coils can be made small to such degree that it does not become a problem in practice.

Further an overlapping part of the solenoid coil to the slot-resonator coil is also constituted by a slender conductor, thereby the coupling between both coils can be further made small.

Since the solenoid coil has the sensitivity in the human body inserting direction and the slot-resonator has the sensitivity in the direction perpendicular to the human body inserting direction, a QD probe can be constituted.

In the vertical-magnetic field type MRI apparatus, low magnetic field intensity of usually 0.05-0.3 tesla or the like is used and the nuclear magnetic resonant frequency also becomes low.

Since inductance is added to the arm section of the slot-resonator coil and therefore the resonant frequency of the slot-resonator coil can be easily lowered, the coil

can be applied to the vertical-magnetic field type MRI apparatus.

Further in the cross coil system where the transmitting and the receiving are performed by separate coils, inductance and capacitance added to the slot-resonator coil constitute a parallel resonant circuit and are controlled to resonate by a switch. As a result, impedance across the added inductance becomes high at the transmitting state and therefore the coupling between the transmitting coil and the slot resonator coil can be cut. If paired diodes are used as this switch, they are turned on at the transmitting state due to application of a large voltage thereby the resonant circuit becomes the resonant state. At the receiving state, since only a small voltage is applied, the paired diodes are at the open state thereby the resonant circuit does not become the resonant state. As a result, the signal receiving can be performed by the slot-resonator coil.

If the overlapping exists at the signal detection portion of the solenoid coil and the slot-resonator coil, the QD probe cannot be constituted. However, when the arm section of the resonator coil is constituted by a slender conductor such as a copper pipe or the like, the overlapping of both coils can be made small hence the coupling between both coils can be made small. Further the overlapping portion for the solenoid coil is also constituted by a slender conductor, thereby the coupling between both coils can be made smaller.

According to the invention, the QD probe can be constituted in the vertical-magnetic field type MR apparatus and the sensitivity uniformity can be improved.

Also since a self-resonant frequency of the slot-resonator coil can be lowered, the resonant frequency of the QD probe can be lowered without deterioration of characteristics.

Further since the coupling between the transmitting coil and the receiving coil in the cross coil system can be avoided, the QD probe can be applied to both the single coil system and the cross coil system.

#### BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a bird's eye view of a QD probe in the prior art;

FIG. 2 is a block diagram of the whole body of a horizontal-magnetic field type MRI apparatus;

FIG. 3 is a diagram showing a constitution of a gradient coil in the horizontal-magnetic field type MRI apparatus of FIG. 2;

FIG. 4 is a block diagram showing a constitution of an electric magnet and parts at its vicinity in a vertical-magnetic field type MRI apparatus;

FIG. 5 is a bird's eye view showing a receiving coil being the main part of an embodiment of the invention;

FIGS. 6(a) and 6(b) are circuit diagrams showing an example of a matching circuit;

FIGS. 7(a) and 7(b) are sectional views along lines VII(a)-VII(a) and VII(b)-VII(b) of FIG. 5, respectively;

FIG. 8 is a bird's eye view showing a receiving coil being the main part of another embodiment of the invention;

FIG. 9 is a circuit diagram showing a part of a receiving coil being the main part of a further embodiment of the invention;

FIGS. 10 and 11 are diagrams illustrating the principle of a cross coil system;

FIG. 12 is a circuit diagram showing a part of a receiving coil being the main part of still another embodiment of the invention;

FIG. 13 is a bird's eye view showing a receiving coil being the main part of still further embodiment of the invention; and

FIG. 14 is a bird's eye view showing a receiving coil being the main part of another embodiment of the invention.

#### DETAILED DESCRIPTION OF EMBODIMENTS

Embodiments of the invention will now be described referring to the accompanying drawings.

FIG. 2 is a block diagram showing an example of a horizontal-magnetic field type MRI apparatus in single coil system where the transmitting and the receiving are performed by one coil. In a vertical-magnetic field type MRI apparatus used in an embodiment of the invention, the direction of a static magnetic field is not horizontal but vertical, however, FIG. 2 will be first described for understanding the MRI apparatus as a whole. A controller 5 outputs various instructions to each of the following units in the definite timing. Output of an RF (radio frequency) pulse generator 6 is amplified by an amplifier 7 and then drives a coil 8. Signal component received by the coil 8 passes through an amplifier 9 and is detected by a detector 10, and then converted into image by a signal processor 11. Gradient magnetic fields in the z-direction and directions perpendicular thereto are generated by coils 12, 13, 14 respectively, and these coils are driven by amplifiers 15, 16, 17 respectively. The static magnetic field is generated by a coil 18, which is driven by a power supply 19. The coil 14 has the same constitution as that of the coil 13, and the coil 14 is rotated by 90 degrees about the z axis with respect to the coil 13 thereby gradient magnetic fields perpendicular to each other are generated. A human body 20 to be inspected is put on a bed 21, which is moved on a supporter 22. FIG. 3 shows an example of constitution of coils generating the gradient magnetic fields in FIG. 2 and direction of current flowing therethrough. In this example, the coil 12 generates the gradient magnetic field in z-axis direction, the coil 13 generates the gradient magnetic field in x-axis direction, and the coil 14 generates the gradient magnetic field in y-direction.

In practice, the coils 12, 13, 14 are used in winding on one cylindrical bobbin.

FIG. 4 is a block diagram showing a constitution example of a vertical-magnetic field type MRI apparatus. A controller 5, an RF pulse generator 6, a detector 10, a signal processor 11, amplifiers 15, 16, 17 and a power supply 19 have the same connection as that in FIG. 2, and therefore are not shown in FIG. 4. FIG. 4 shows a cross coil system where the transmitting and the receiving are performed by separate coils. In the cross coil system, the output of the RF pulse generator 6 is amplified by an amplifier 7 and then excites a transmitting coil 81. A signal component received by a receiving coil 82 passes through an amplifier 9 and is detected by the detector 10. A detailed constitution example of coils 12, 13, 14 generating the gradient magnetic fields shall be omitted here. In FIG. 4, the coils 12, 13, 14 generating the gradient magnetic fields are drawn simplifying in one coil.

FIG. 5 is a constitution diagram of a receiving coil being the main part of an embodiment of the invention. In the embodiment, a slot-resonator coil is wound on the outside of a solenoid coil 102 (In FIG. 5, a bobbin of

insulating material supporting the solenoid coil 102 is not shown.). In the slot-resonator coil, signal electrodes 103, 104 in the form of conductive arms are wound on upper and lower guard rings 105, 106 through an insulator (not shown in FIG. 5). Among the signal electrodes 103, 104, an opposed portion (called a wing) to the guard rings 105, 106 is connected by capacitors 107, 108, 109, 110. In the case of FIG. 5, the sensitivity of the solenoid coil is in the z-axis direction and the sensitivity of the slot-resonator coil is in the x-axis direction. That is, if the static magnetic field is taken in the y-axis direction, a QD probe can be constituted in combination of the solenoid coil and the slot-resonator coil. Consequently, the sensitivity uniformity in the signal detecting can be improved. Although a matching circuit leading to feeding points C and D is not shown in FIG. 5, a matching circuit by capacitors 201, 202 shown in FIG. 6(a) or FIG. 6(b) may be used.

However, both the solenoid coil and the slot-resonator coil are designed so as to resonate in the desired resonant frequency.

FIGS. 7(a) and 7(b) are sectional views taken along lines VII(a)-VII(a) and VII(b)-VII(b) of FIG. 5, respectively. In FIGS. 7(a) and 7(b), a bobbin 130 of insulating material with a solenoid coil 102 wound thereon and an insulation layer 131 between a guard ring 105 and a wing are specifically shown. As shown in FIG. 7(a), the guard ring 105 and the wing portion of the signal electrode 103 are opposed through the insulation layer 131. Also capacitors 107, 108 are connected between the wings.

In the vertical-magnetic field type MRI apparatus, in general, the nuclear magnetic resonant frequency is low, but since the slot-resonator coil is suitable for the operation at high frequency, when it is used in the vertical magnetic field type MRI apparatus, lowering of the resonant frequency without deteriorating the characteristics may become a problem. The settling measure will be described as follows.

FIG. 8 shows an embodiment of constitution where one arm section of the slot-resonator coil of the QD probe for the vertical-magnetic field type MRI apparatus shown in FIG. 5 is divided and has an inductance 150 added thereto. When the inductance 150 is added as shown in FIG. 8, the self-resonant frequency of the slot-resonator coil can be lowered thereby the resonant frequency of the QD probe can be lowered without deteriorating the characteristics.

Also in the case of the cross coil system as shown in FIG. 4 where the transmitting and the receiving are performed in separate coils, the coupling between the transmitting coil and the receiving coil becomes a problem.

The coupling between the transmitting coil and the receiving coil in the cross coil system will be described. Now, the position relation in each coil is noticed and simplification is performed as shown in FIG. 10. In FIG. 10, a coil 210 represents a solenoid coil of FIG. 8, and a coil 200 represents a slot-resonator coil of FIG. 8. A coil 220 represents a transmitting coil. The position relation of the coils 200, 210, 220 becomes the position shown in FIG. 10 or FIG. 11 (the coil 220 being in parallel to the coil 200 or the coil 210) in practice. (Existence of the transmitting direction within the xz plane is possible from the principle of NMR, but the position relation in practice becomes as shown in FIG. 10 or FIG. 11 from the position relation with the human body inserting direction or the receiving coil.)

In FIG. 10, the sensitivity direction of the solenoid coil 210 is in the z-axis direction and the sensitivity direction of the slot-resonator coil 200 is in the x-axis direction, and the transmitting direction of the transmitting coil 220 is in the x-axis direction. Consequently, a large signal transmitted from the transmitting coil 220 is inputted directly to the slot-resonator coil 200. Also a problem of the coupling occurs that the slot-resonator coil becomes an inductive load for the transmitting coil 220. In the arrangement in FIG. 11, a similar problem of the coupling occurs between the transmitting coil 220 and the solenoid coil 210.

FIG. 9 shows the decoupling means for solving the problem of the coupling between the transmitting coil and the slot-resonator coil produced by the arrangement of FIG. 10. That is, the signal electrode 104 of the slot-resonator coil shown in FIG. 8 is divided, and the inductance 150 is added thereto and further a capacitor 160 and paired diodes 170 are added in parallel to the inductance 150. Since the large voltage is applied across the inductance 150 during the transmitting, the paired diodes 170 are rendered conductive. If the paired diodes 170 become conductive, the inductance 150 and the capacitor 160 constitute the resonant circuit and the impedance across the inductance 150 becomes large, thereby the signal electrode 104 becomes equivalent to the cut state apparently. If the signal electrode 104 is cut, the slot-resonator coil become an open loop and therefore does not become an inductive load of the transmitting coil 220 and the transmitting signal is not inputted. On the other hand, since only a small voltage is applied across the inductance 150 during the receiving, the paired diodes 170 become non-conductive thereby the inductance 150 and the capacitor 160 do not constitute the resonant circuit. Consequently, the signal electrode 104 becomes non-cut state and acts as the slot-resonator coil and receives signals.

Next, FIG. 12 shows the decoupling means for solving the problem of the coupling between the solenoid coil 210 and the transmitting coil 220 produced in the case of the arrangement shown in FIG. 11. As shown in FIG. 12, the solenoid coil 210 is divided by capacitors 211-217. By dividing the solenoid coil 210 by the capacitors 211-217, the influence during the human body inserting can be reduced. When the solenoid coil is divided by the capacitors in such manner, for example, inductance 218 and paired diodes 219 are connected in parallel to the capacitor 214 and the resonant circuit is constituted, thereby the coupling with the transmitting coil can be avoided in similar manner to the above-mentioned principle.

When the solenoid coil and the slot-resonator coil are combined, the coupling occurs between both coils and a problem of deterioration of the performance as the QD coil occurs. When the solenoid coil and the slot resonator coil are combined, it is characterized in that the overlapping in the signal detection section is small and the mutual influence is small. However, the mutual influence can be further reduced by following manner. That is, as shown in FIG. 13, among the signal electrodes of the slot-resonator coil, a part for substantially receiving signals (a part in parallel to the z-axis, called an "arm") is constituted by a slender conductor such as a copper rod and the like. Then since the width of the arm affects the sensitivity distribution during the receiving, as shown in FIG. 13, the two arm units are constituted by copper rods 300, 301 or 302, 303, each in two rods. In this constitution, the signal detection can be

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performed without changing the arm width substantially.

Further as shown in FIG. 14, a portion at the side of the solenoid coil opposed to the arm unit is thinned, thereby the coupling between the solenoid coil and the slot-resonator coil can be further reduced.

We claim:

1. A nuclear magnetic resonance imaging apparatus comprising:

static magnetic field generation means for generating a static magnetic field in a cylindrical space having an axis along a first direction, said static magnetic field generation means generating said static magnetic field in a second direction perpendicular to the first direction;

a quadrature-phase detection probe for detecting a high-frequency magnetic field caused by nuclear magnetic resonance in said cylindrical space, said quadrature-phase detection probe including a slot-resonator coil and a solenoid coil;

said slot-resonator coil having two conductive arms extending in parallel to the axis of said cylindrical space and positioned on opposite sides of the axis of said cylindrical space so as to be spaced apart from each other in the second direction, one of said two conductive arms having ends thereof capacitively coupled to corresponding ends of the other of said two conductive arms so that said slot-resonator coil has a sensitivity enabling detection of a high-frequency magnetic field component in a third direction perpendicular to the first and second directions; and

said solenoid coil including a coil member wound around a circumference of said cylindrical space so that said solenoid coil has a sensitivity enabling detection of a high-frequency magnetic field component in the first direction.

2. A nuclear magnetic resonance imaging apparatus according to claim 1, wherein at least one of said two conductive arms of said slot-resonator coil is divided into two parts, and further comprising an inductance connecting the divided parts.

3. A nuclear magnetic resonance imaging apparatus according to claim 1, further comprising:

high-frequency magnetic field generation means for generating a high-frequency magnetic field in the third direction perpendicular to the first and second directions in the cylindrical space; and decoupling means providing in a current path in said slot-resonator coil for enabling decoupling.

4. A nuclear magnetic resonance imaging apparatus according to claim 3, wherein said decoupling means includes a series circuit of a capacitor and a switching element, and an inductance connected in parallel with said series circuit, said capacitor and said inductance resonating at a frequency of said high-frequency mag-

netic field generated by said high-frequency magnetic field generation means when said inductance enables coupling to said capacitor through said switching element.

5. A nuclear magnetic resonance imaging apparatus according to claim 4, wherein said switching element includes a pair of diodes connected in parallel to each other and having polarities opposite to each other, said pair of diodes presenting a low impedance under a voltage induced by said high-frequency magnetic field generated by said high-frequency magnetic field generation means and being in a non-conductive state under a voltage induced by said high-frequency magnetic field generated by said nuclear magnetic resonance.

6. A nuclear magnetic resonance imaging apparatus according to claim 1, wherein a portion of at least one of said coil member of said solenoid coil and at least one of said conductive arms of said slot-resonator coil at overlapped portions of said coil member and said at least one of said conductive arms is thinner in comparison with other portions thereof.

7. A nuclear magnetic resonance imaging apparatus according to claim 1, wherein each of said two conductive arms includes at least one slender conductor.

8. A nuclear magnetic resonance imaging apparatus according to claim 7, wherein said slender conductor is a copper rod.

9. A nuclear magnetic resonance imaging apparatus according to claim 1, further comprising:

high-frequency magnetic field generation means for generating a high-frequency magnetic field in the first direction in the cylindrical space; and decoupling means provided in a current path in said solenoid coil for enabling decoupling.

10. A nuclear magnetic resonance imaging apparatus according to claim 9, wherein said decoupling means includes a series circuit of an inductance and a switching element, and a capacitor connected in parallel with said series circuit, said capacitor and said inductance resonating at a frequency of said high-frequency magnetic field generated by said high-frequency magnetic field generation means when said capacitor enables coupling to said inductance through said switching element.

11. A nuclear magnetic resonance imaging apparatus according to claim 10, wherein said switching element includes a pair of diodes connected in parallel to each other and having polarities opposite to each other, said pair of diodes presenting a low impedance under a voltage induced by said high-frequency magnetic field generated by said high-frequency magnetic field generation means and being in a non-conductive state under a voltage induced by said high-frequency magnetic field caused by said nuclear magnetic resonance.

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